

Compal Confidential

Model Name : Z5WAH

File Name : LA-B161P

Compal Confidential

EA50_HB M/B Schematics Document

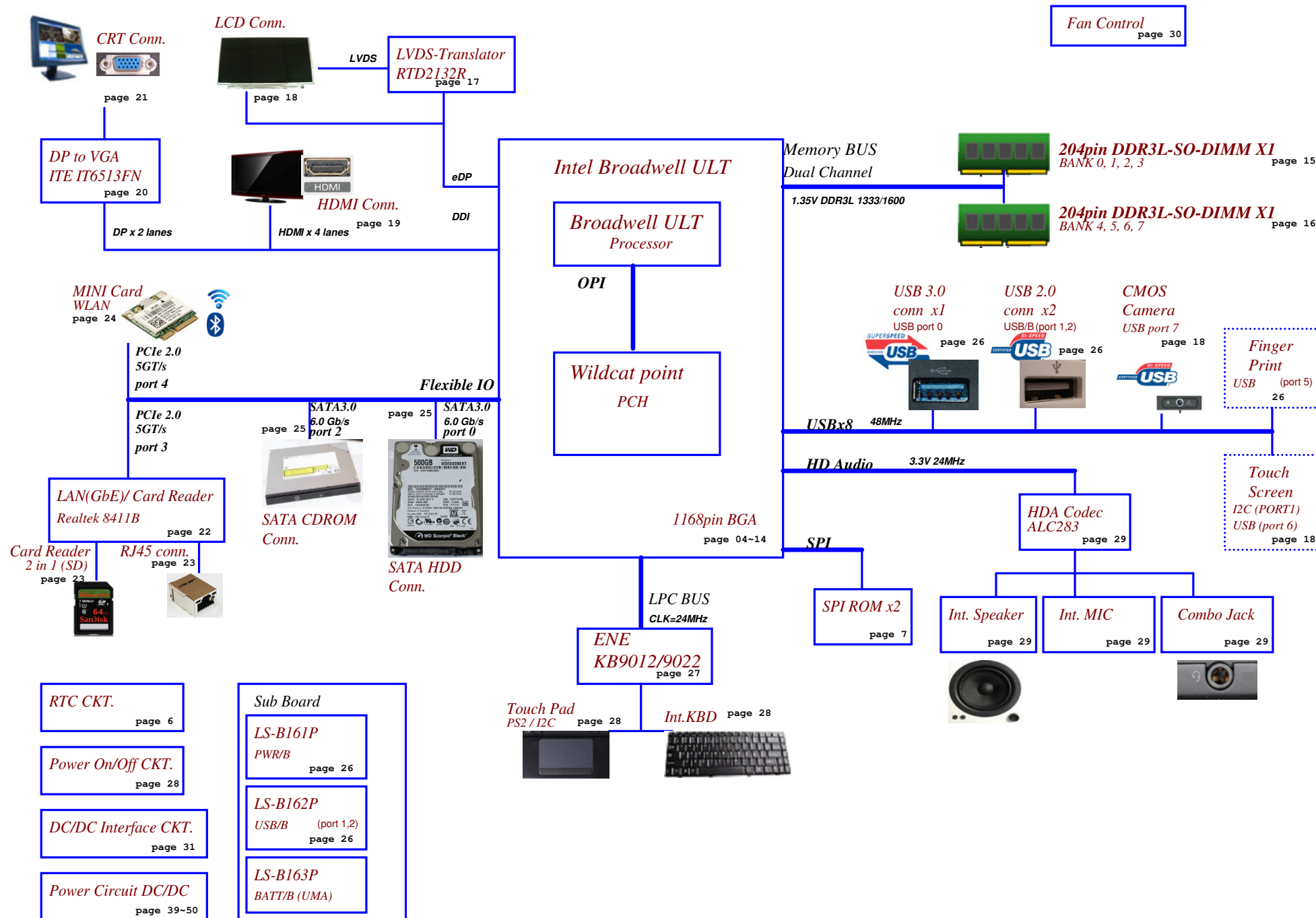
Intel Broadwell ULT (Broadwell + Wildcat point)

2014-03-04

REV : 1 . 0

For 20140225 pre-MP gerber

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2013/10/30	Deciphered Date	2014/10/30	Title Cover Page	
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Issued Date	2013/10/30	Deciphered Date	2014/10/30	Block Diagrams	
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Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.675VS	+0.675VS power rail for DDR3L terminator	ON	OFF	OFF
+1.05VS_VTT	+1.05V power rail for CPU	ON	OFF	OFF
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+1.5VS	+1.5V power rail for CPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VLP	B+ to +3VLP power rail for suspend power	ON	ON	ON
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VS	+5VALW to +5VS power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X	On Board Thermal Sensor	0100 110x
		VGA Internal Thermal Sensor	0100 000x
		G Sensor	0011 000x

Device		Address	
ChannelA	DIMM0	1001 000x	JDIMM1
ChannelB	DIMM1	1001 010x	JDIMM2

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0 V	0 V	0 V
1	12K +/- 5%	0.347 V	0.354 V	0.360 V
2	15K +/- 5%	0.423 V	0.430 V	0.438 V
3	20K +/- 5%	0.541 V	0.550 V	0.559 V
4	27K +/- 5%	0.691 V	0.702 V	0.713 V
5	33K +/- 5%	0.807 V	0.819 V	0.831 V
6	43K +/- 5%	0.978 V	0.992 V	1.006 V
7	56K +/- 5%	1.169 V	1.185 V	1.200 V
8	75K +/- 5%	1.398 V	1.414 V	1.430 V
9	100K +/- 5%	1.634 V	1.650 V	1.667 V
10	130K +/- 5%	1.849 V	1.865 V	1.881 V
11	160K +/- 5%	2.015 V	2.031 V	2.046 V
12	200K +/- 5%	2.185 V	2.200 V	2.215 V
13	240K +/- 5%	2.316 V	2.329 V	2.343 V

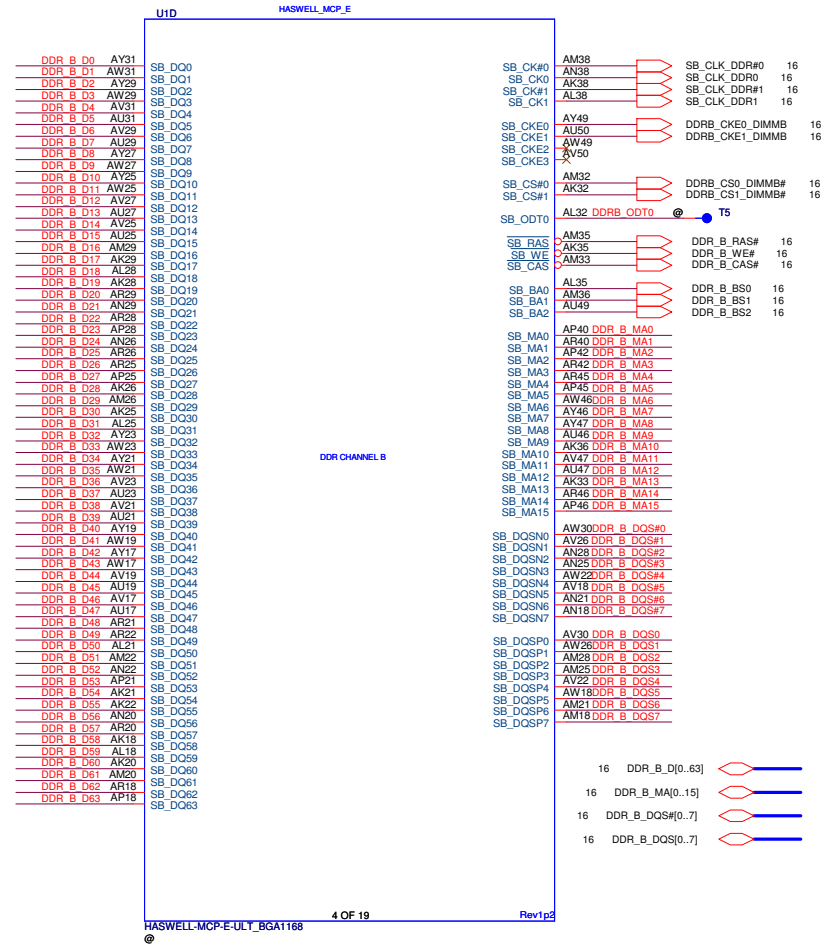
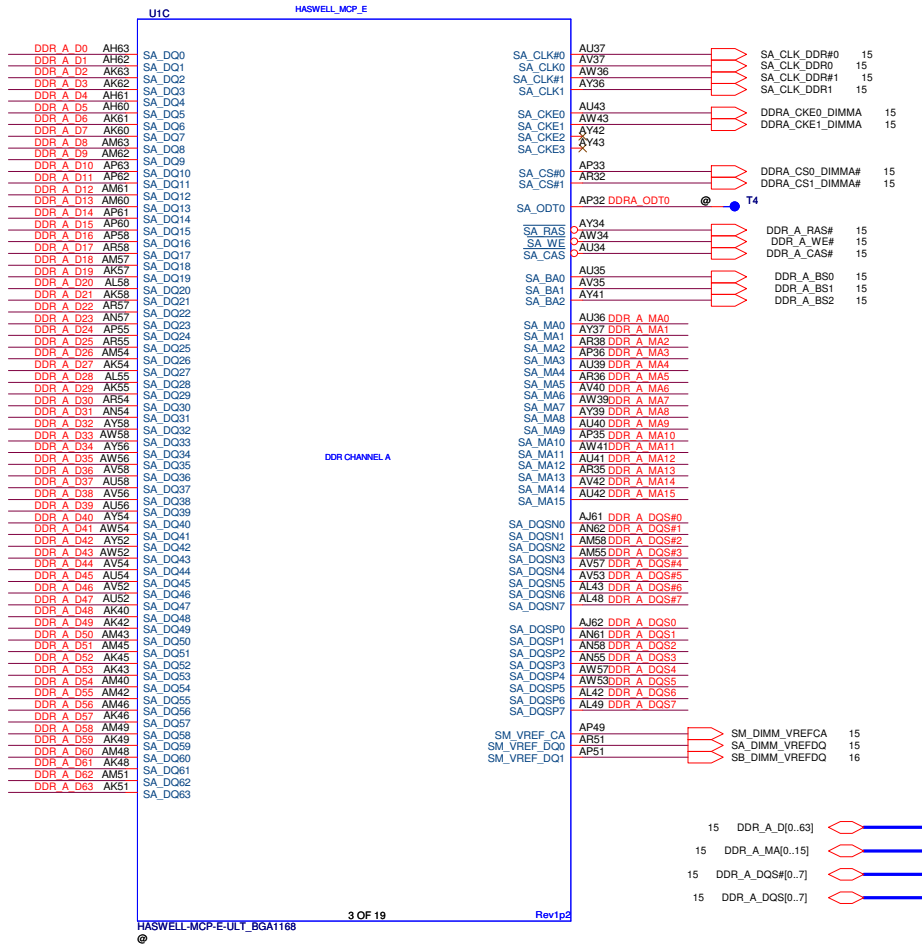
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

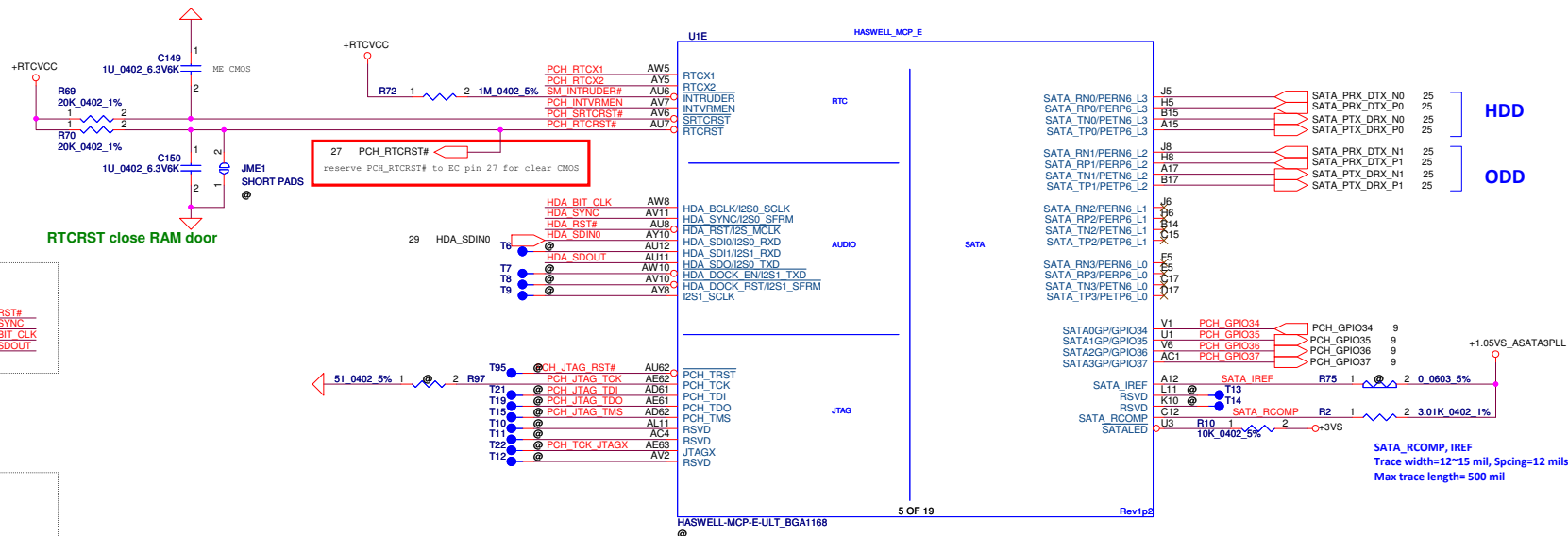
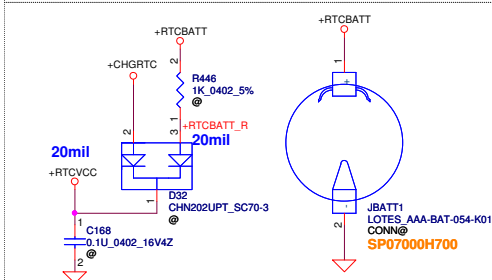
USB 2.0	Port	3 External USB Port
EHCI1	0	USB Port(Left 3.0)
	1	USB Port(Right 2.0)
	2	USB Port(Right 2.0)
	3	
	4	Mini Card (WLAN+BT)
	5	Finger Print
	6	Touch Screen
	7	Camera

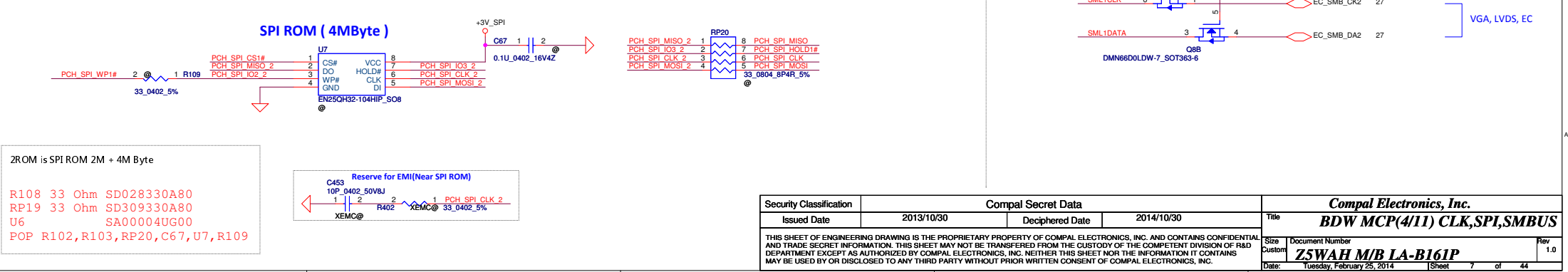
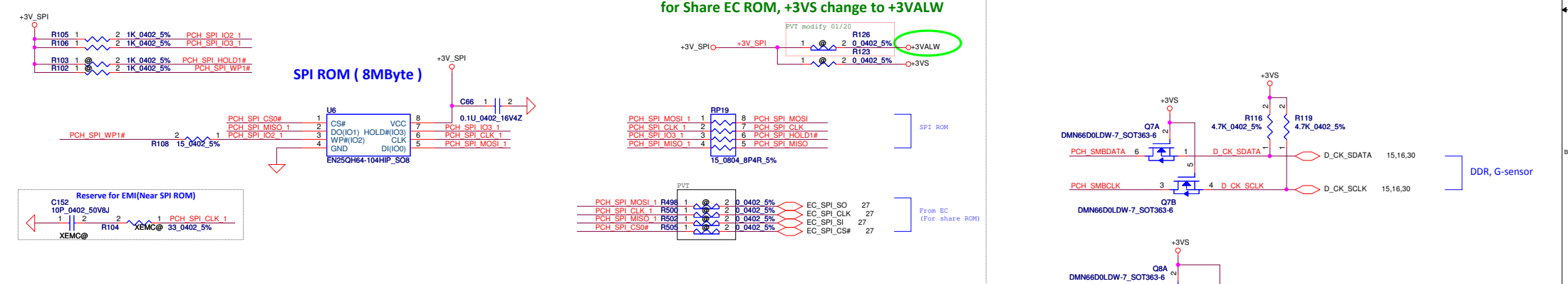
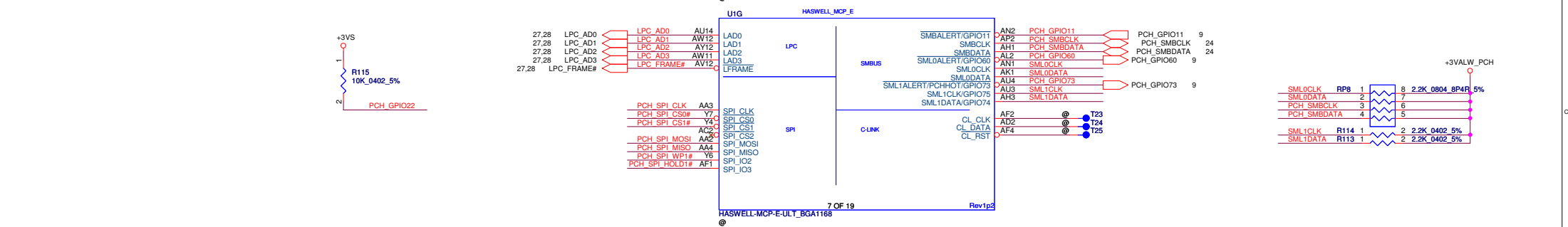
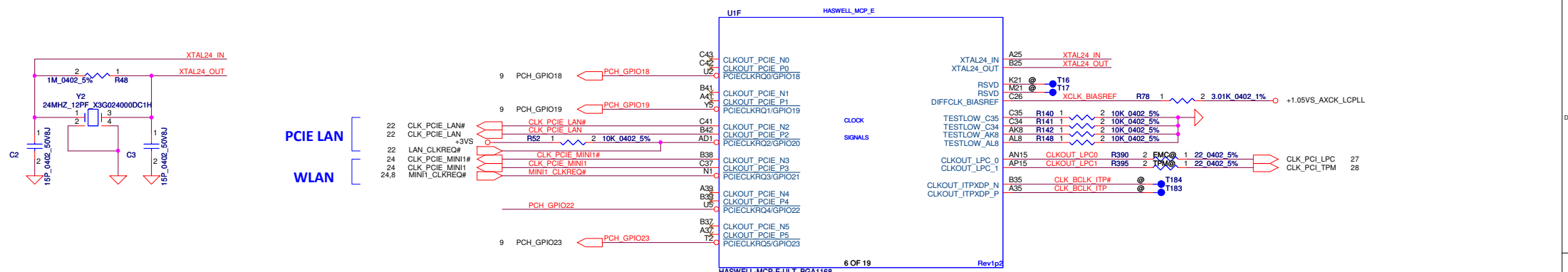
USB 3.0	Port	
XHCI	0	USB Port(Left 3.0)
	1	
	2	
	3	

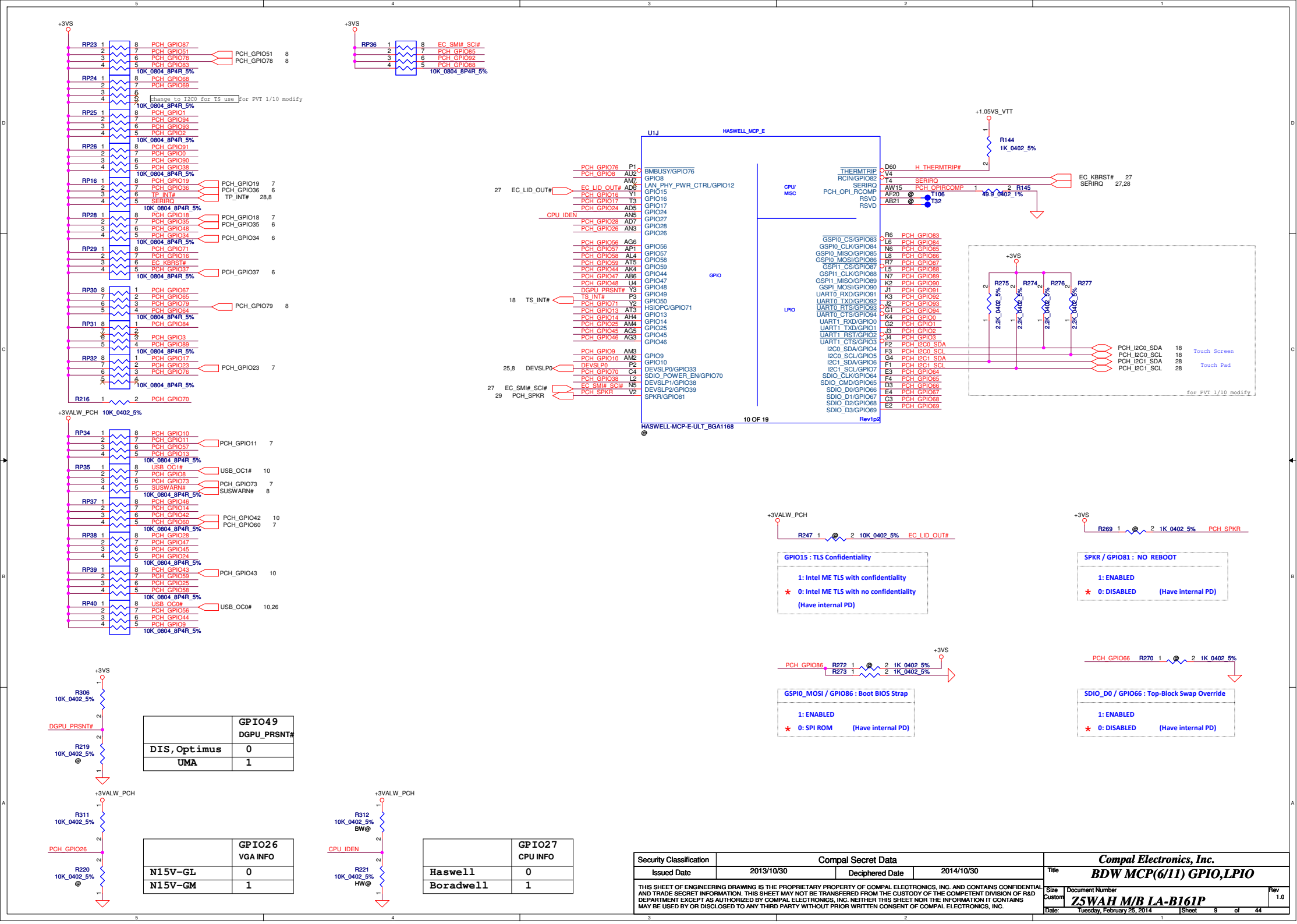
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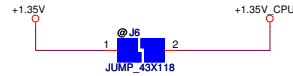
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Issued Date	2013/10/30	Deciphered Date	2014/10/30	Title	Notes List	
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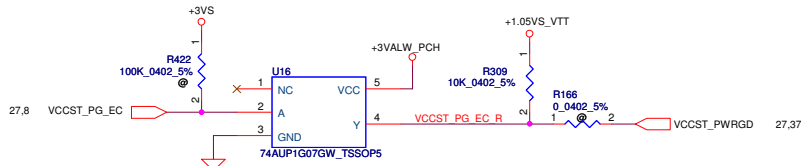




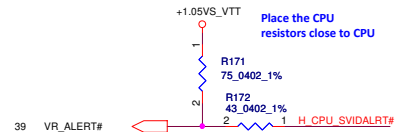




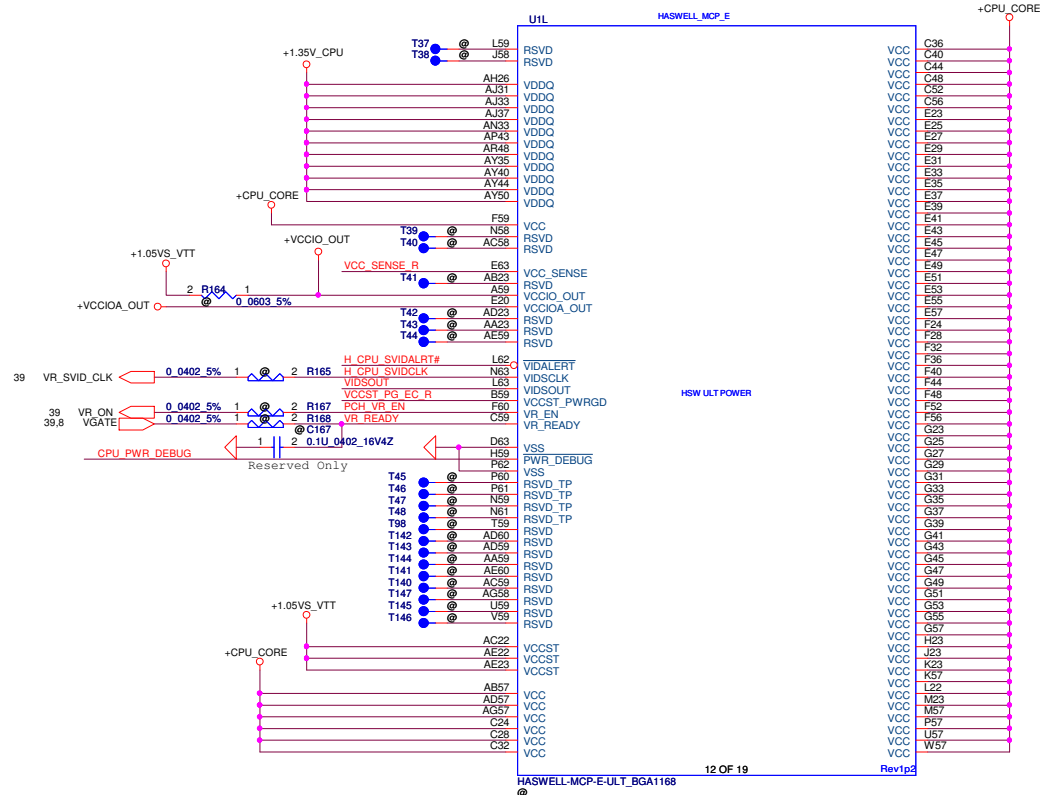
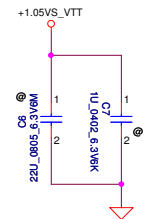
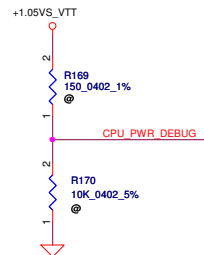
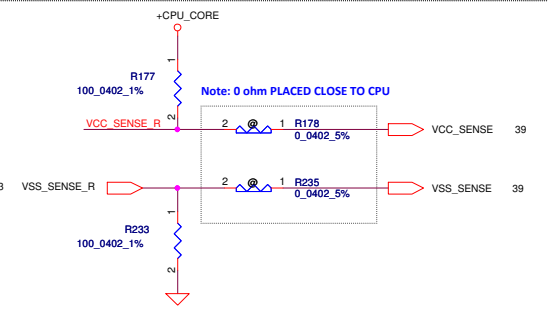
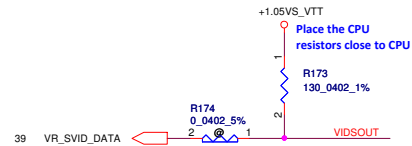
Shark Bay ULT have internal gate for VDDQ



SVID ALERT

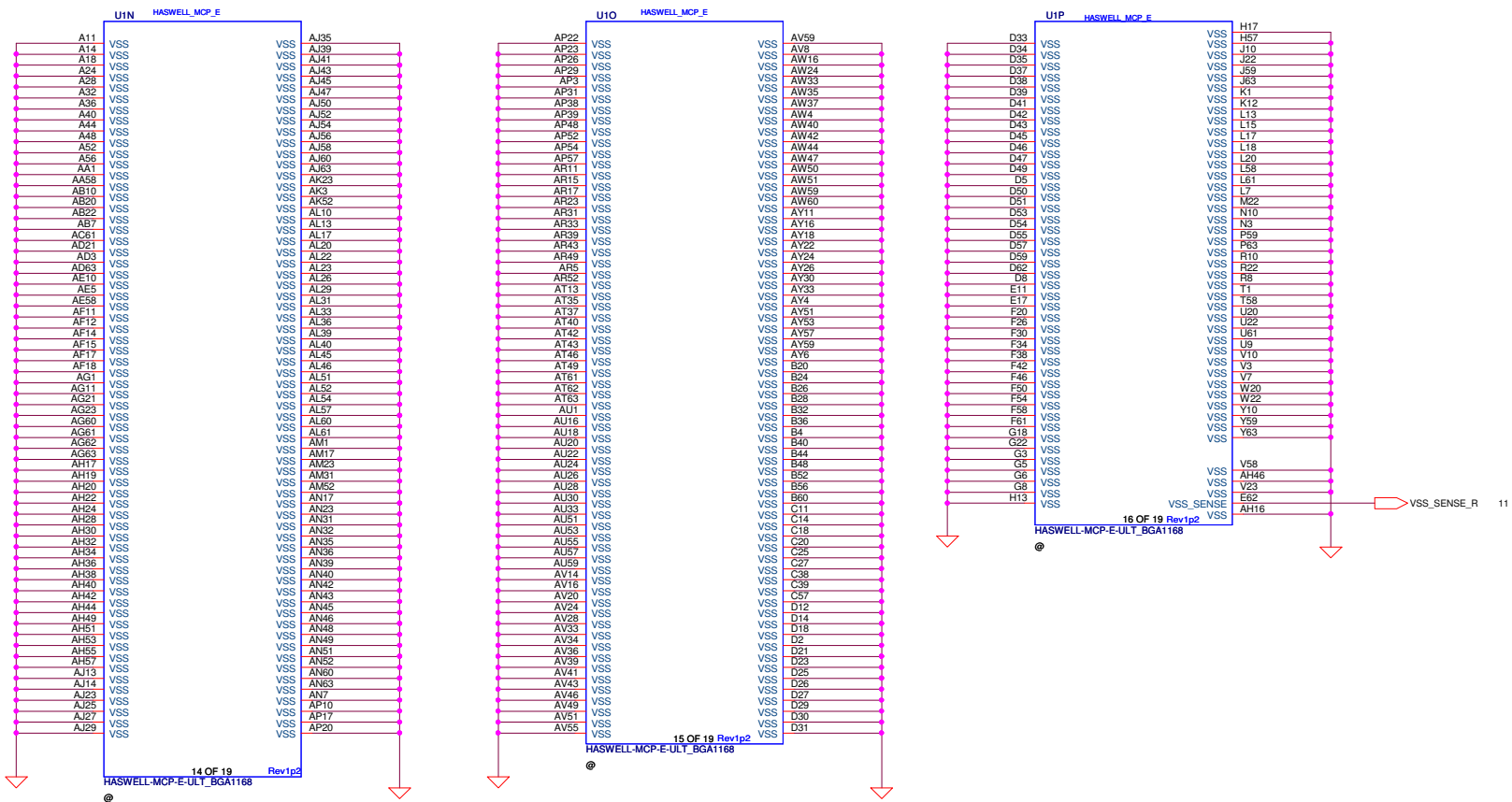


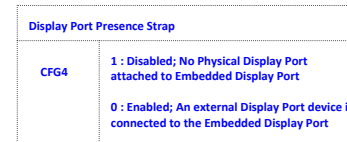
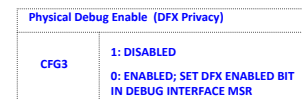
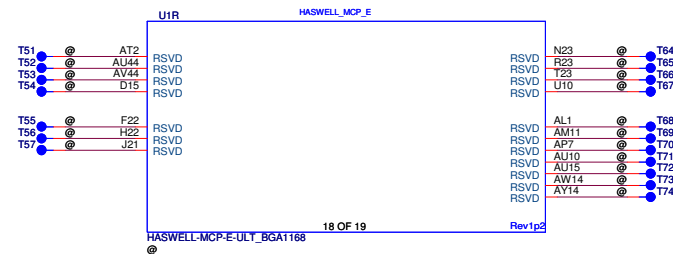
SVID DATA

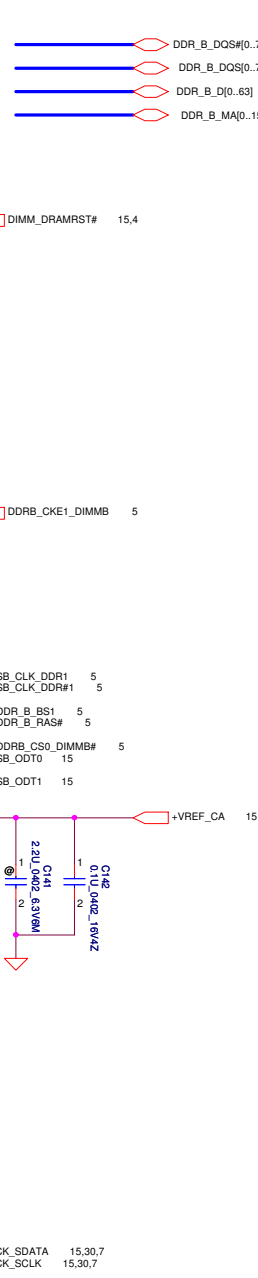


+1.35V : 470UF/2V/7343 * 2
10UF/6.3V/0603 * 6
2.2UF/6.3V/0402 * 4

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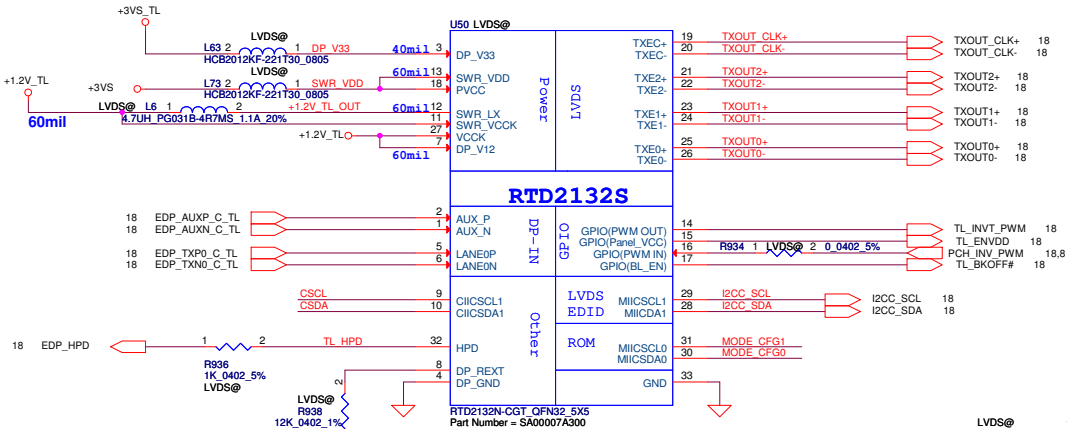
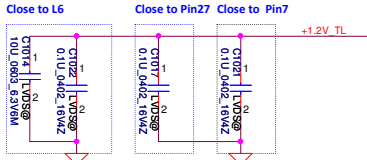
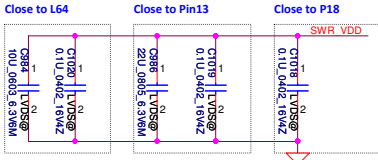
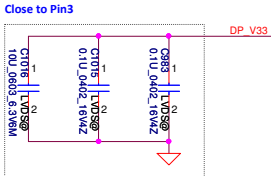
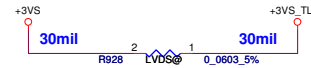




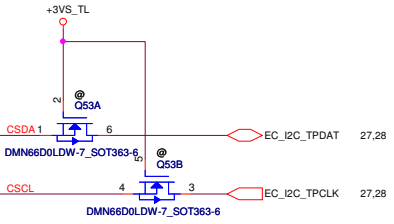
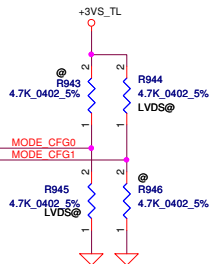
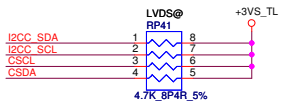


<Address: SA1:SA0=10>
DIMM_2 H:4mm
DIS for Standard type
UMA for Reverse type

LVDS Translator - RTD2132R



use 2132S symbol



MODE_CFG0(PIN30)		
	0	1
MODE_CFG1(PIN31)	X	EP MODE
	ROM ONLY MODE*	EEPROM MODE

WWW.AliSaler.Com

The schematic shows the power management section of the G624T11U_SOT23-5. It includes two DC-DC converters:

- W=60mils Converter:** A buck converter with input from +3VS through capacitor C140 (1u_0402_6.3VXK). The output is connected to the EN pin of U8 (G624T11U_SOT23-5) and also passes through capacitor C367 (4.7U_0603_6.3V6K) and inductor L40DVIDD before reaching the +L40DVIDD output.
- INVT PWM Converter:** An inverting buck-boost converter using U20 (M74VHC1GT125DF2G_SC70-5). Its input is connected to +3VS through resistor R362 (100K_0402_5%). The output INVT PWM is connected to the TL_INV_TPM pin of the TL module.

Other components include resistors R947 (FDR@ 2 0 0.0402 5%), R950 (LVDS@ 2 0 0.0402 5%), R383 (EDP@ 2 0 0.0402 5%), R404 (@ 2 0 0.0402 5%), R405 (LVDS@ 2 0 0.0402 5%), R393 (100K_0402_5%), and R401 (1K_0402_5%). Signal pins PCH_INV_PWM, EDP_DISP_UTIL, and TL_INV_TPM are shown at the bottom.

The schematic diagram illustrates the EDP connector pinout for the Intel Atom C3000 series. It shows the following connections:

- EDP_TXN0 (Pin 4):** Connected to C372 (1) and C371 (1). C372 (1) is connected to EDP@ 0.1U 0402 16V7K EDP TXN0 C. C371 (1) is connected to EDP@ 0.1U 0402 16V7K EDP TXP0 C.
- EDP_TXP0 (Pin 4):** Connected to C377 (1) and C376 (1). C377 (1) is connected to 2 LVDS@0.1U 0402 16V7K EDP TXN0 C TL. C376 (1) is connected to 2 LVDS@0.1U 0402 16V7K EDP TXP0 C TL.
- EDP_TXN1 (Pin 4):** Connected to C374 (1).
- EDP_TXP1 (Pin 4):** Connected to C373 (1).
- EDP_AUXN (Pin 4):** Connected to C369 (1) and C370 (1). C369 (1) is connected to EDP@ 0.1U 0402 16V7K EDP AUXN C. C370 (1) is connected to EDP@ 0.1U 0402 16V7K EDP AUXP C.
- EDP_AUXP (Pin 4):** Connected to C388 (1) and C389 (1). C388 (1) is connected to 2 LVDS@0.1U 0402 16V7K EDP_AUXN_C_TL. C389 (1) is connected to 2 LVDS@0.1U 0402 16V7K EDP_AUXP_C_TL.
- CPU_EDP_HPD (Pin 8):** Connected to R406 (1) and R406 (2). R406 (1) is connected to EDP_HPD. R406 (2) is connected to EDP_HPD.
- EDP_HPD (Pin 17):** Connected to R364 (1) and R364 (2). R364 (1) is connected to EDP_HPD. R364 (2) is connected to EDP_HPD.

The diagram also shows a +3VS connection to the EDP_AUXN and EDP_AUXP pins, and a ground connection to the EDP_HPD pin.

[illegible]

Pin-to-pin connection diagram for the E-T_0871K-F40N-00L connector. The diagram shows two rows of pins, 1-11 on the left and 12-40 on the right. Various signals are connected to specific pins, including power (W=60mils), LCD data (LCDVDD), touch screen data (TS_EN1, TS_RST#, TS_INT#), and camera data (USB20_P5 CAMERA, USB20_N5 CAMERA). A green label 'SP01001120' is at the bottom right.

Pin Connections:

- Pin 1:** +INVPWR_B_
- Pin 2:** W=60mils
- Pin 3:** W=60mils
- Pin 4:** INVTPWM
- Pin 5:** DISPOFF#
- Pin 6:** EDP_HPD
- Pin 7:** +LCDVDD
- Pin 8:** TS_EN1
- Pin 9:** TXOUT_CLK_
- Pin 10:** TXOUT_CLK_
- Pin 11:** TXOUT2_
- Pin 12:** TXOUT2_
- Pin 13:** TS_RST#
- Pin 14:** TXOUT1_
- Pin 15:** TXOUT1_
- Pin 16:** TXOUT0_
- Pin 17:** TXOUT0_
- Pin 18:** EDID_I2C_SDA
- Pin 19:** EDID_I2C_SCL
- Pin 20:** +3VS
- Pin 21:** EDP_AUXN_C
- Pin 22:** EDP_AUXP_C
- Pin 23:** EDP_TXP0_C
- Pin 24:** EDP_TXN0_C
- Pin 25:** EDP_TXP1_C
- Pin 26:** EDP_TXN1_C
- Pin 27:** TS_INT#
- Pin 28:** TS_INT#
- Pin 29:** USB20_P5
- Pin 30:** USB20_N5
- Pin 31:** USB20_P5 CAMERA
- Pin 32:** USB20_N5 CAMERA
- Pin 33:** +3VS
- Pin 34:** USB20_P5 CAMERA
- Pin 35:** USB20_N5 CAMERA
- Pin 36:** +3VS
- Pin 37:** USB20_P5 CAMERA
- Pin 38:** USB20_N5 CAMERA
- Pin 39:** +3VS
- Pin 40:** USB20_P5 CAMERA

Labels:

- Touch Screen:** TS_EN1, TS_RST#, TS_INT#, TXOUT_CLK_, TXOUT2_, TXOUT1_, TXOUT0_.
- For Camera:** USB20_P5 CAMERA, USB20_N5 CAMERA.

Other Labels: W=60mils, INVTPWM, DISPOFF#, EDP_HPD, +LCDVDD, +3VS, EDP_AUXN_C, EDP_AUXP_C, EDP_TXP0_C, EDP_TXN0_C, EDP_TXP1_C, EDP_TXN1_C, USB20_P5, USB20_N5.

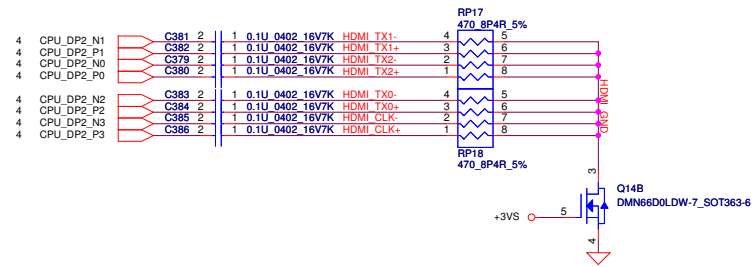
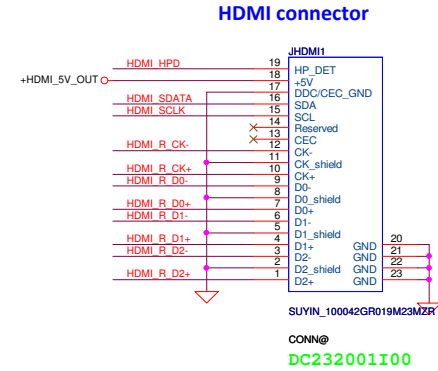
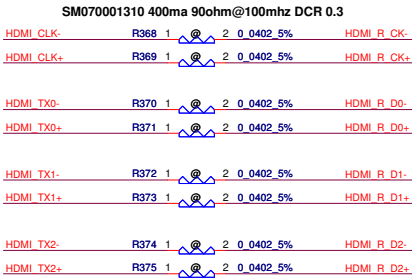
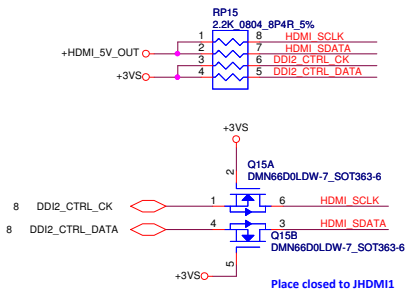
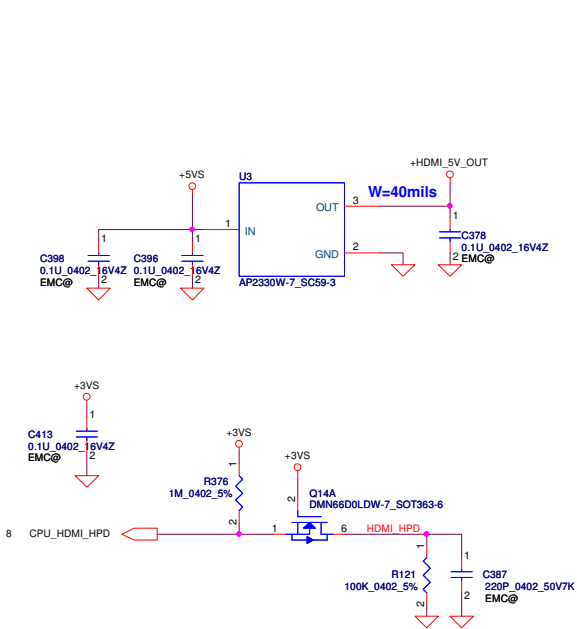
Bottom Right: E-T_0871K-F40N-00L CONN@, SP01001120

pin define, conn need to confirm

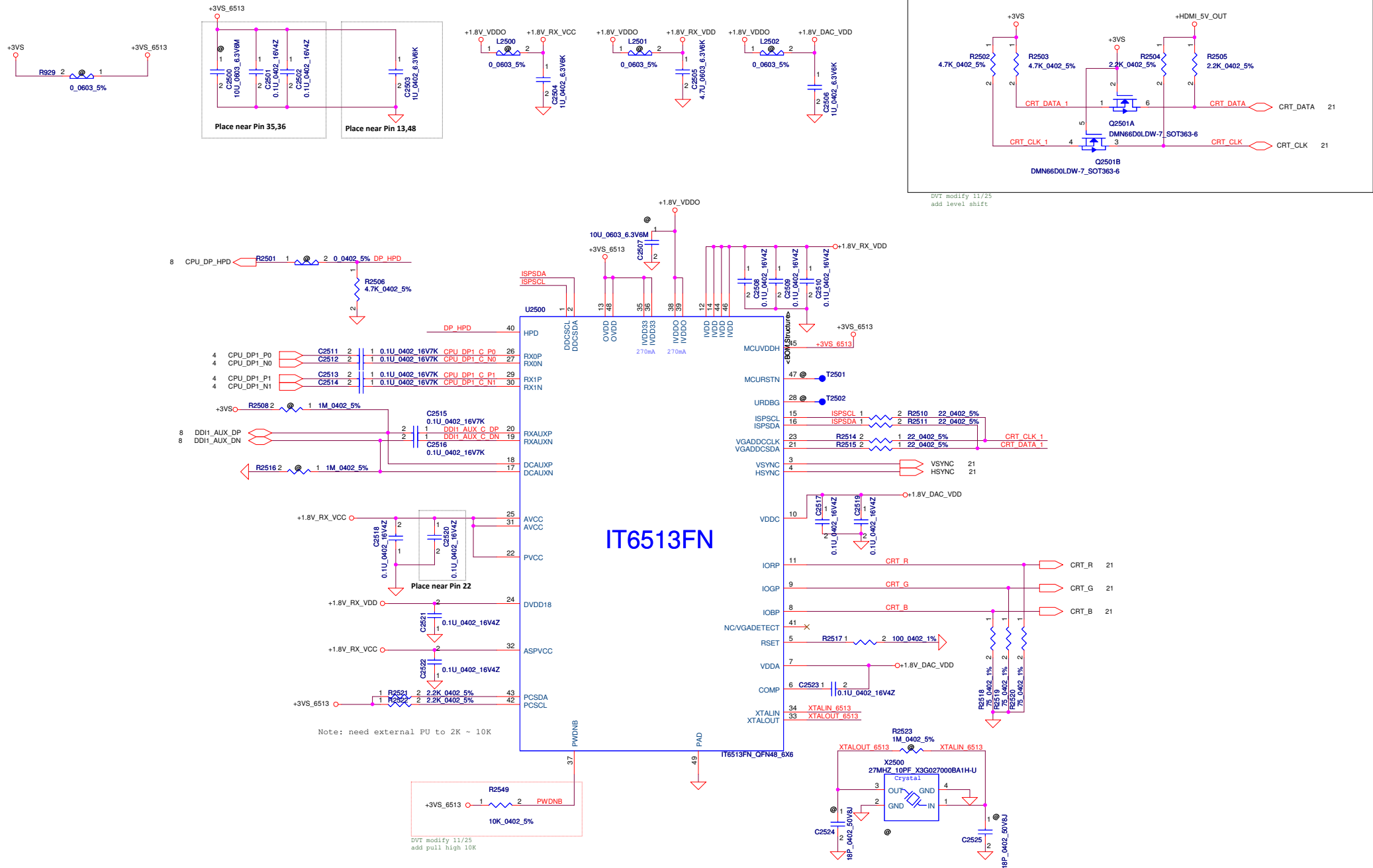
SP02000K200

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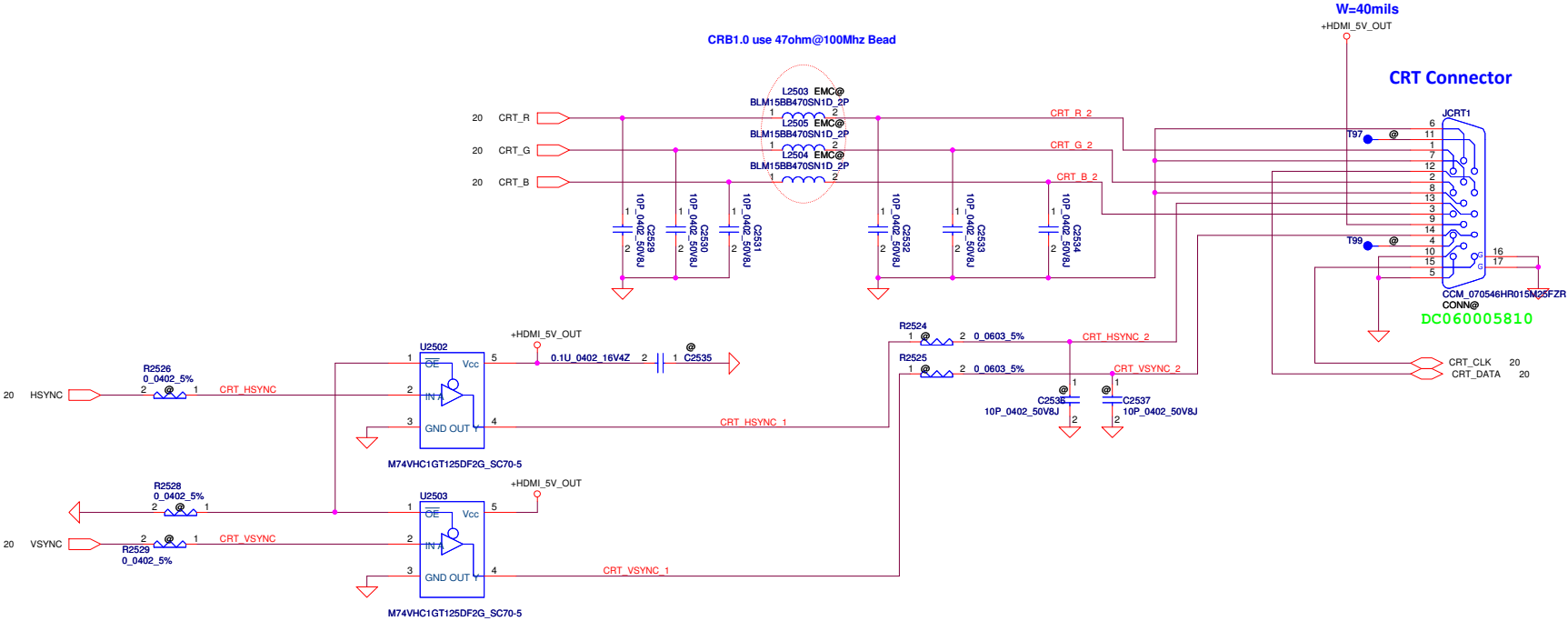
HDMI conn.



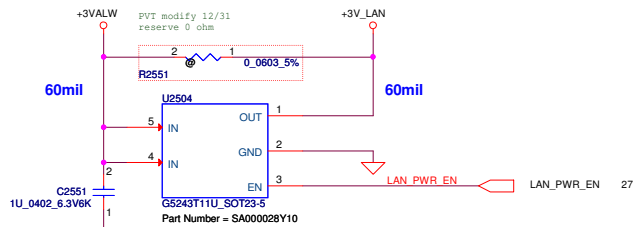
DP to VGA-IT6513



CRT conn.



LAN-RTL8411B

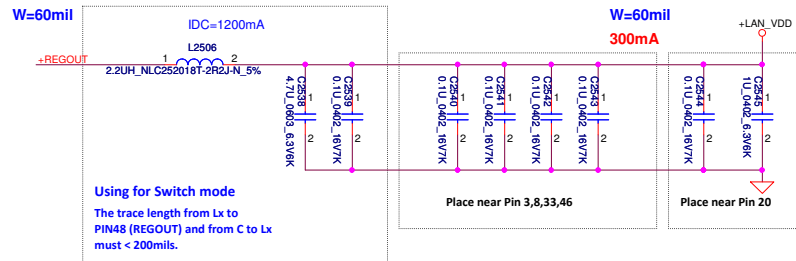


From EC
High active.
EN threshold voltage min:1.2V typ:1.6V max:2.0V
Current limit threshold 1.5~2.8A
+3V_LAN Rising time must >0.5ms and <100ms

EC_PME# pull high 10K to +3VALW

PU at PCH side
C788,C791
Place near Pin 25,26

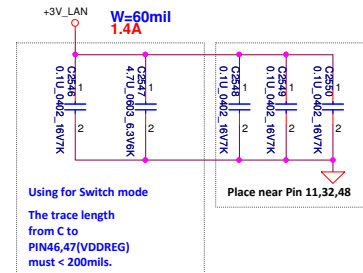
W=60mil



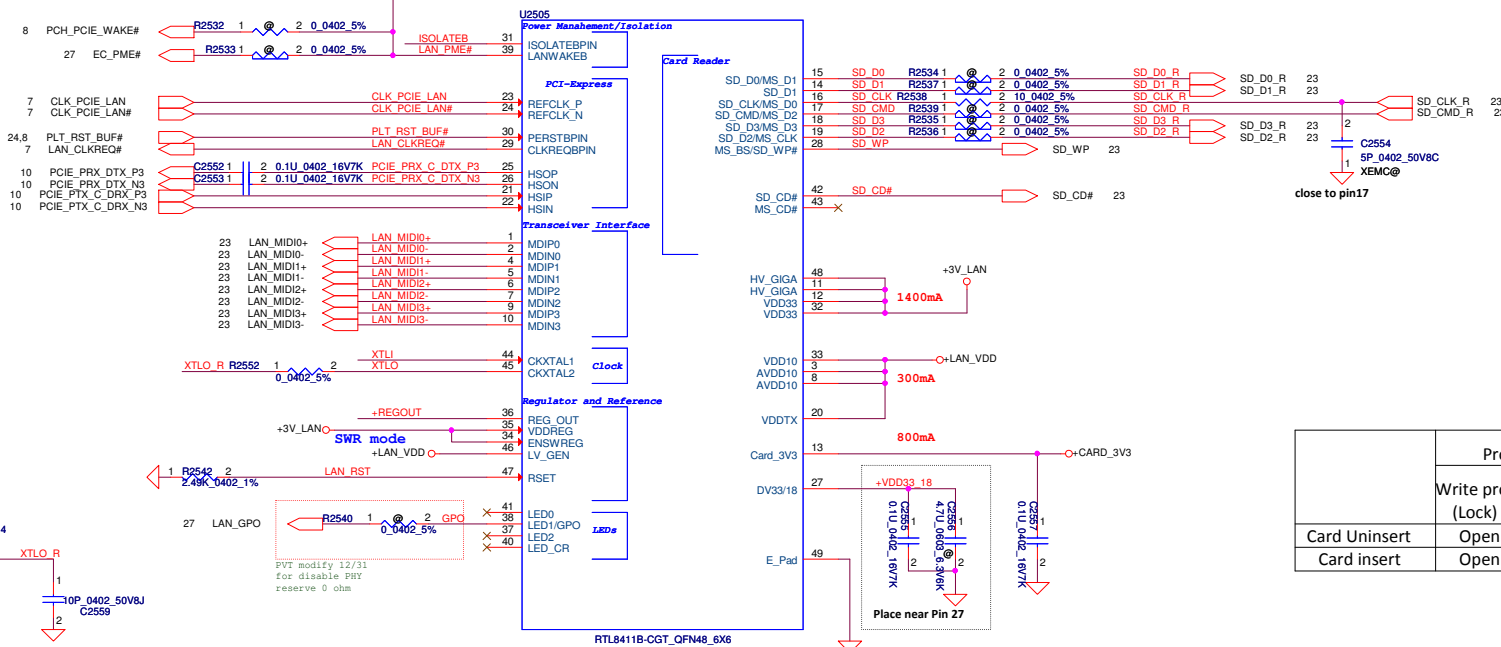
Using for Switch mode
The trace length from Lx to PIN48 (REGOUT) and from C to Lx must < 200mils.

W=60mil
300mA

W=60mil
1.4A

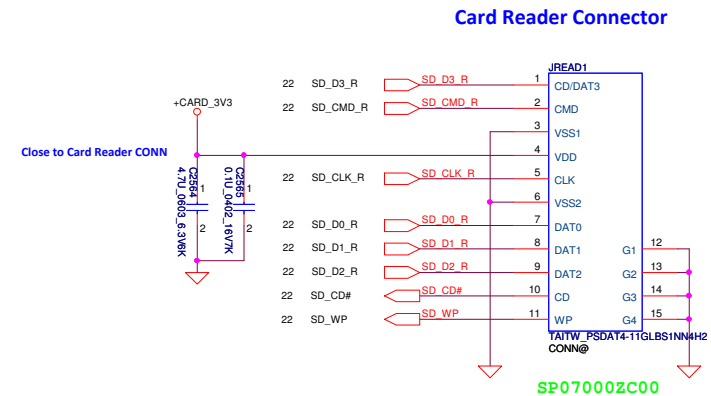
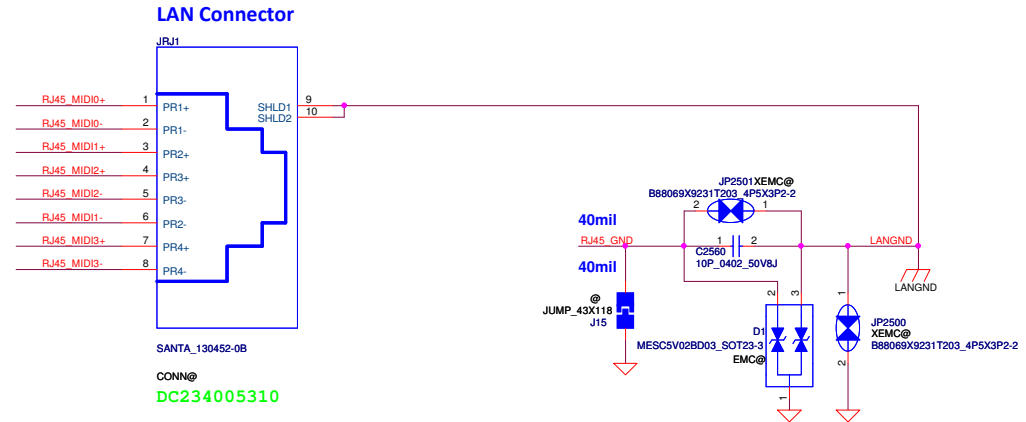
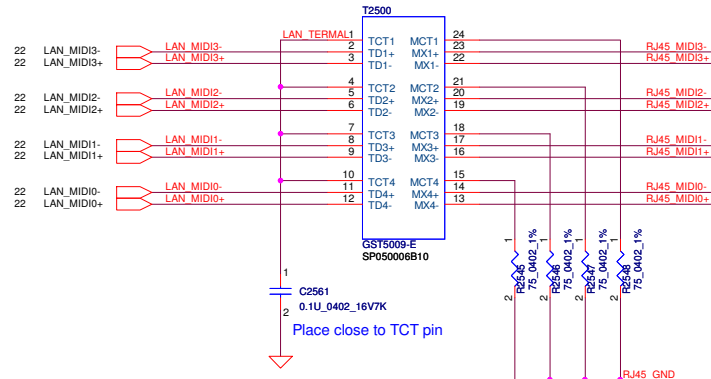


Using for Switch mode
The trace length from C to PIN46,47(VDDREG) must < 200mils.



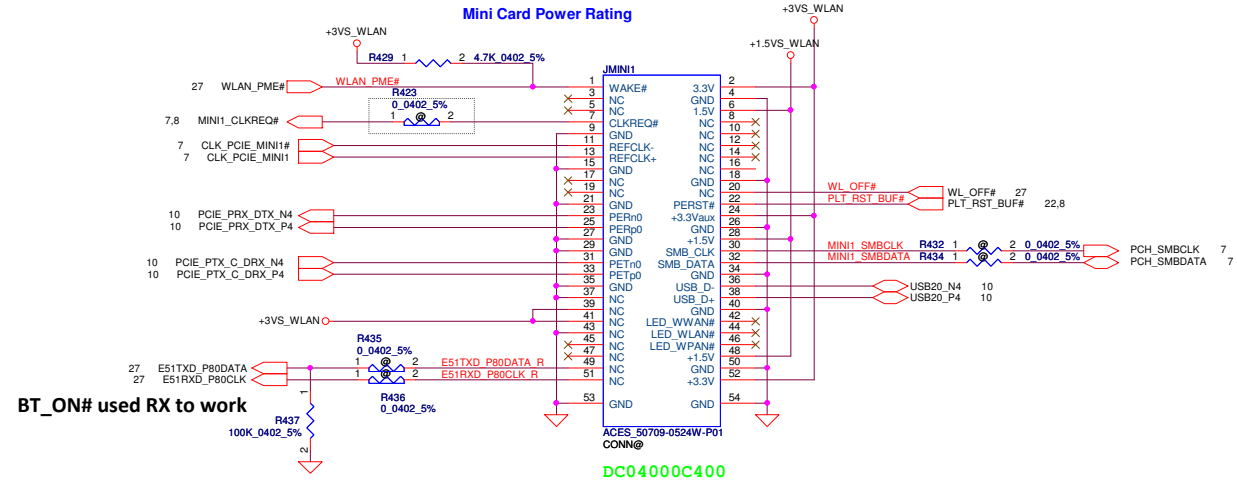
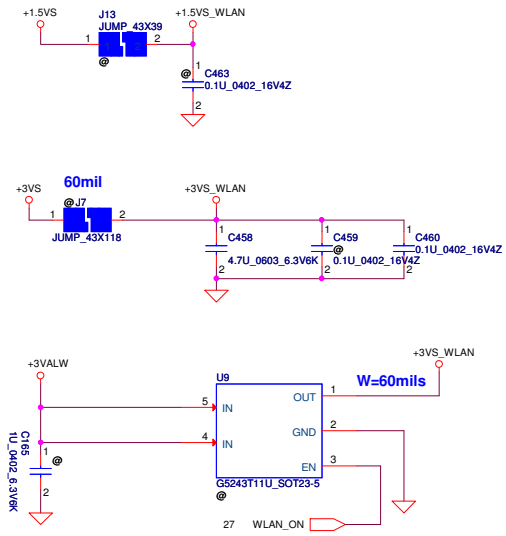
	Protect cotact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close

RJ45 / Card Reader conn.

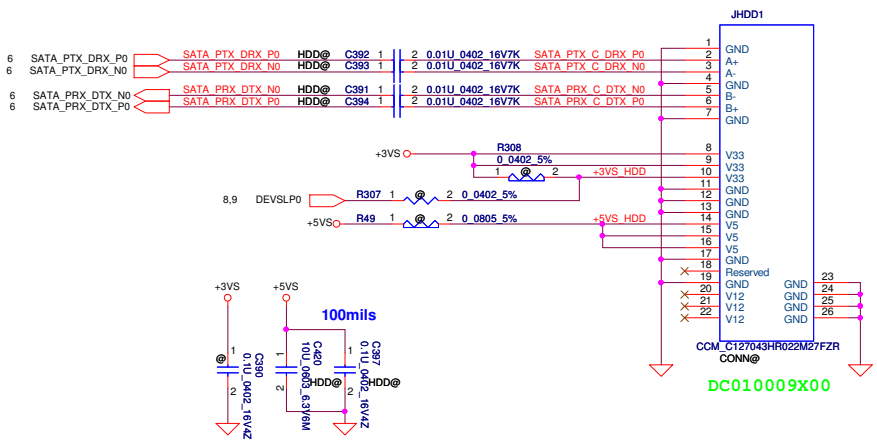


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				Custom	Z5WAH M/B LA-B161P	1.0
				Date:	Tuesday, February 25, 2014	Sheet 23 of 44

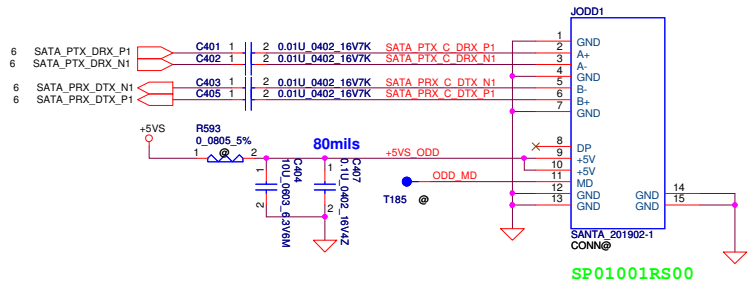
Wireless LAN



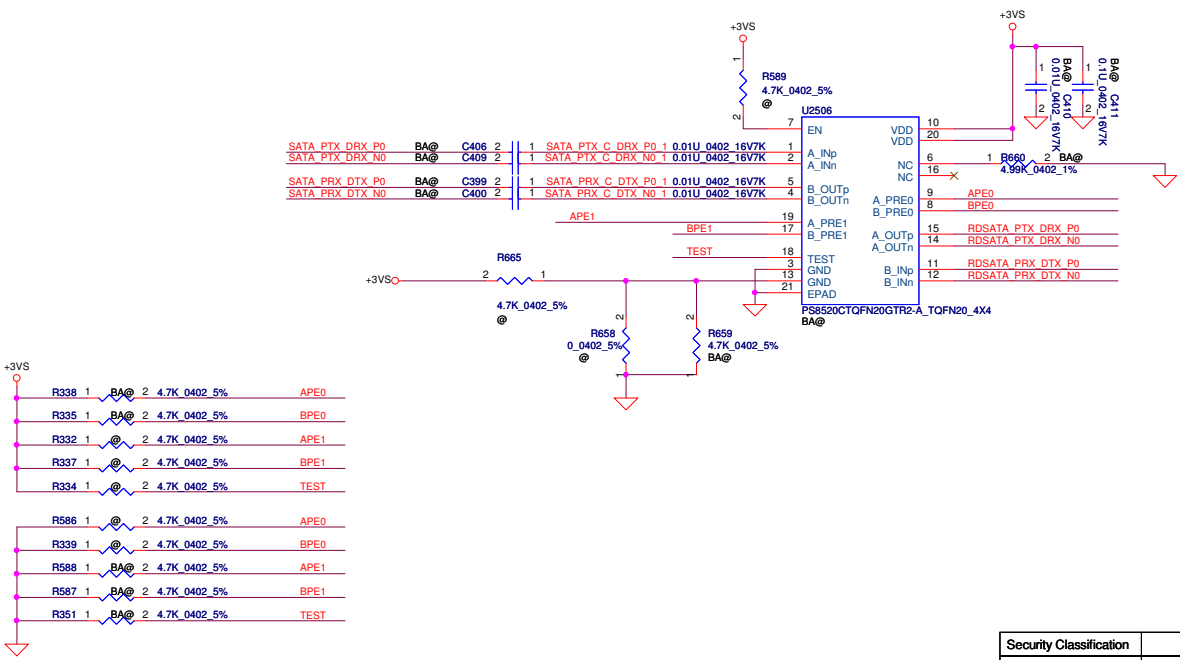
SATA HDD1 Conn.



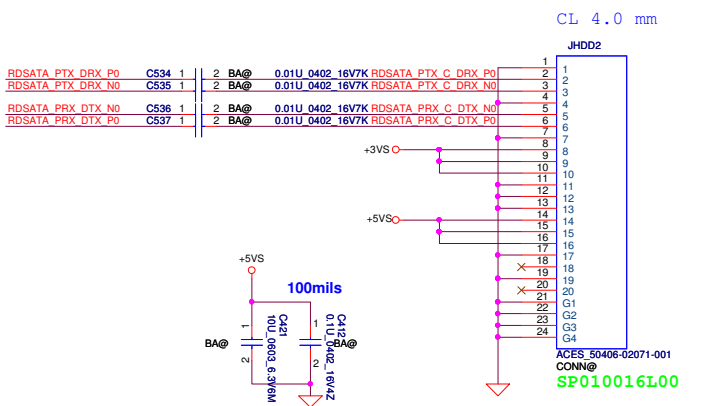
SATA ODD Conn.



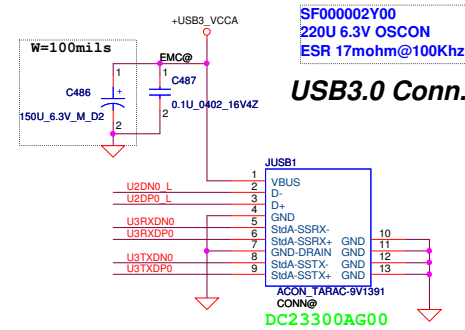
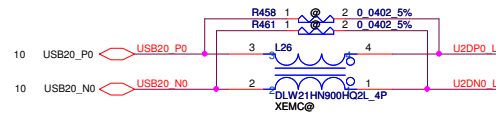
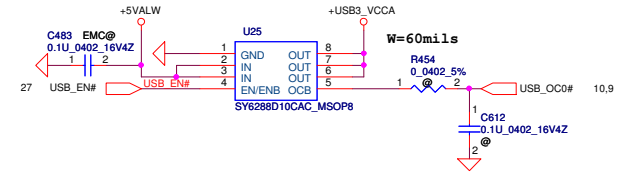
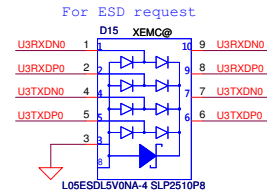
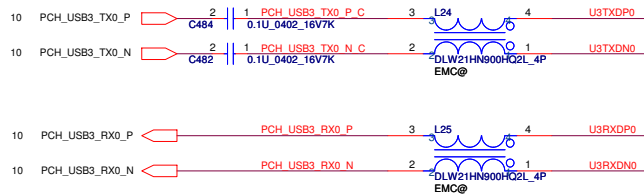
SATA Re-Driver HDD Conn. Reserve



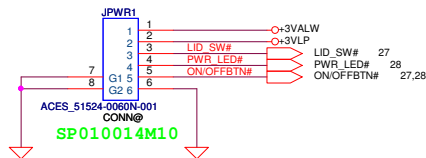
SATA HDD1 Conn.



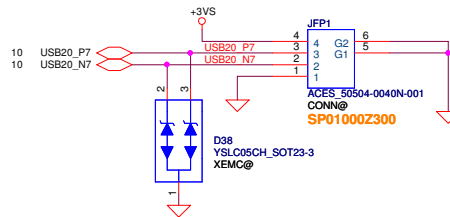
USB3.0 (Port 0)



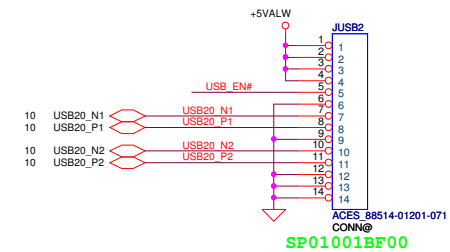
PWR/B

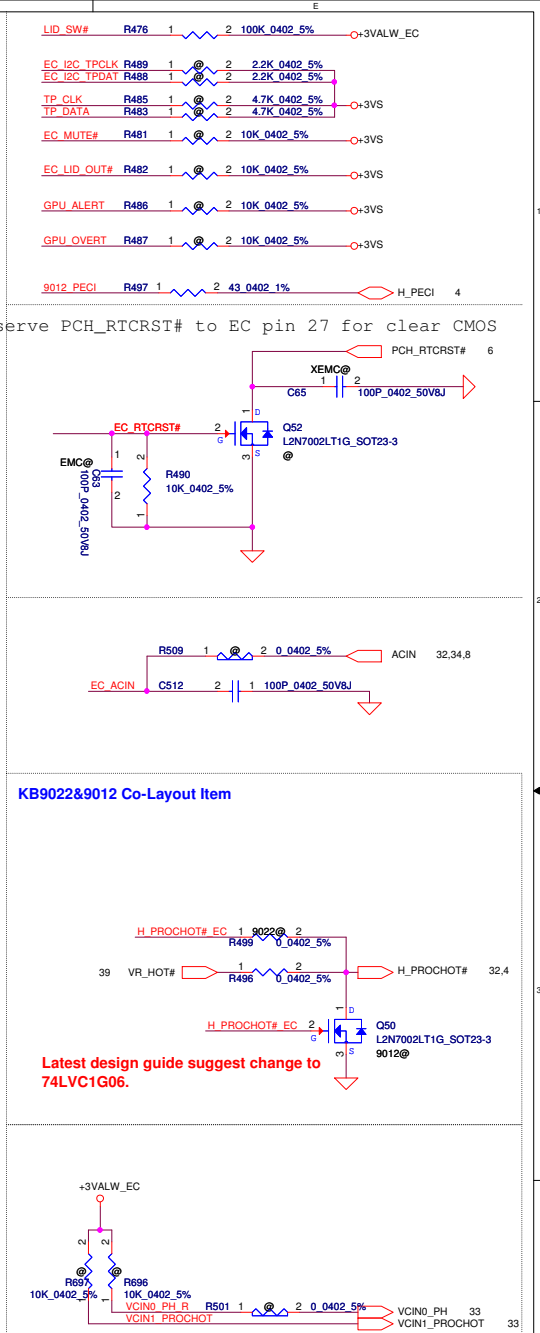
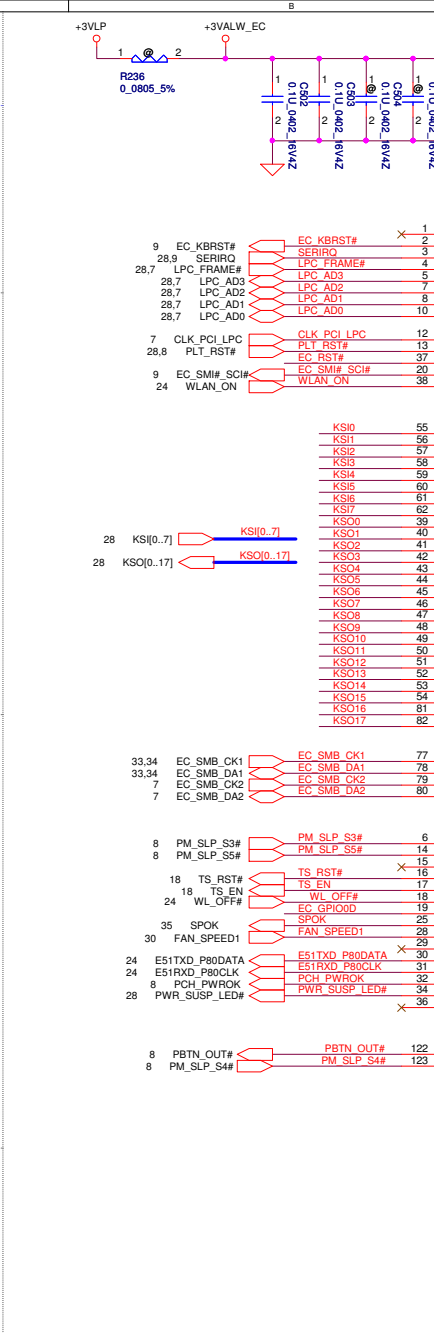


Finger Print /B Reserve



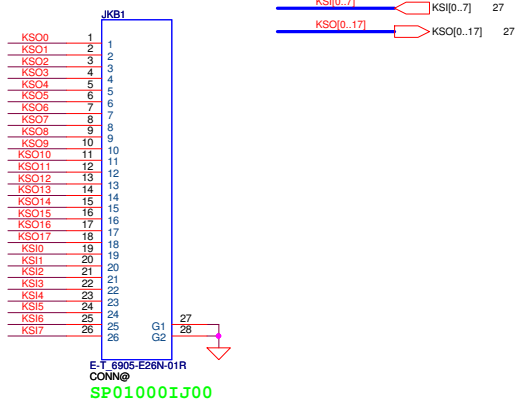
USB/B (USB Port 1, Port2)



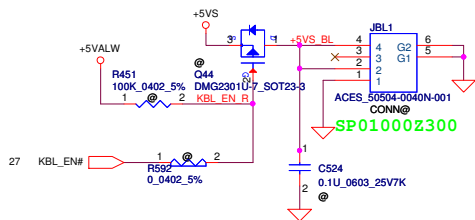


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KB Conn.

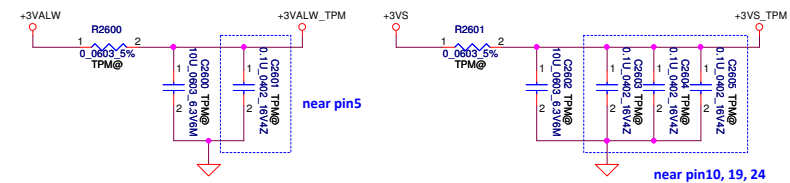


KB BackLight Conn. Reserve

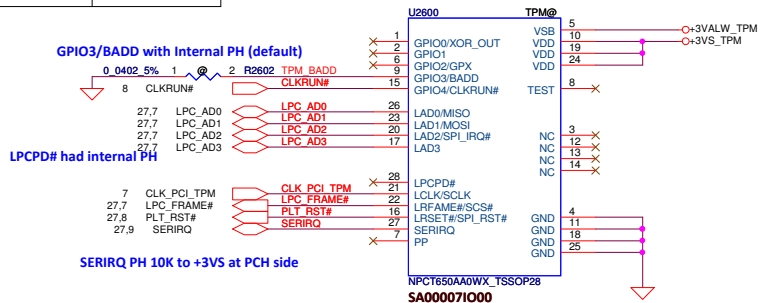


TPM Board for 2015

for PVT 1/14 modify

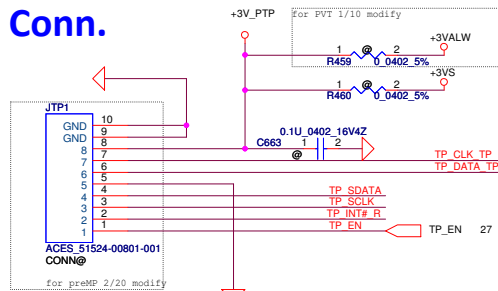


BADD	SELECTION
0	EEh - EFh
* 1	7Eh - 7Fh



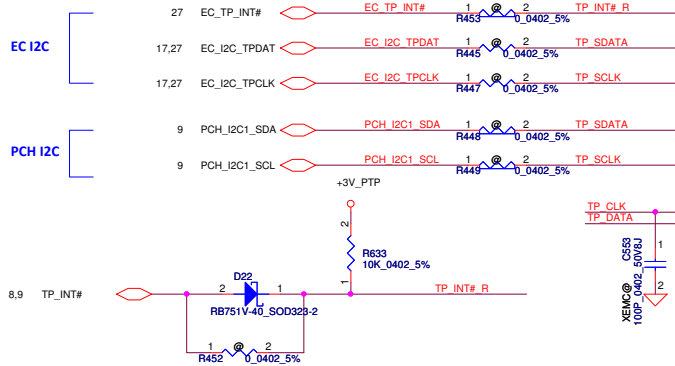
CLK_PCI_TPM R2603 1 2 33 0402 5% C2606 1 2 22P 0402 50V6J

TP/B Conn.

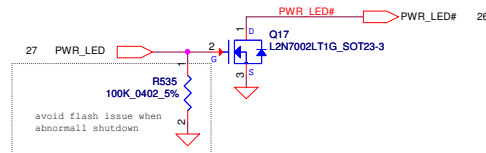


EC I2C

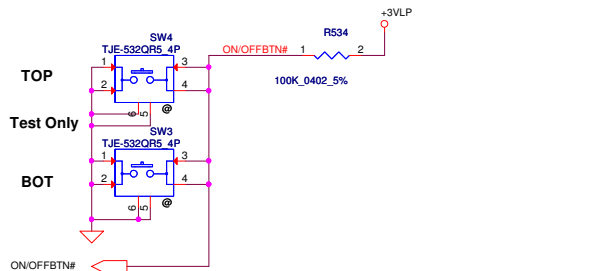
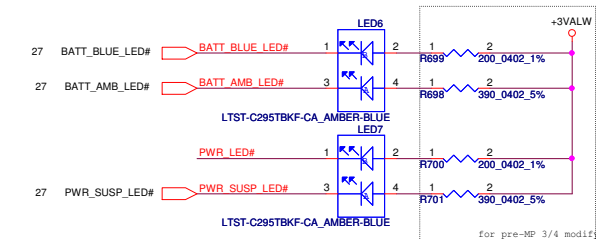
PCH I2C



LED

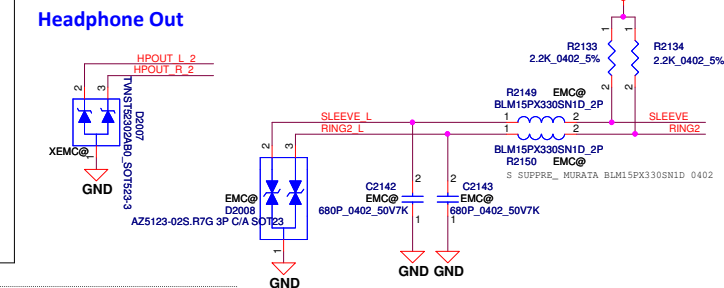
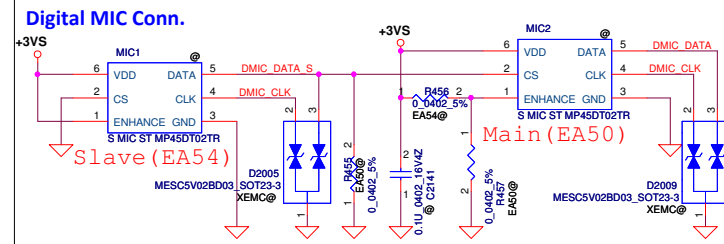
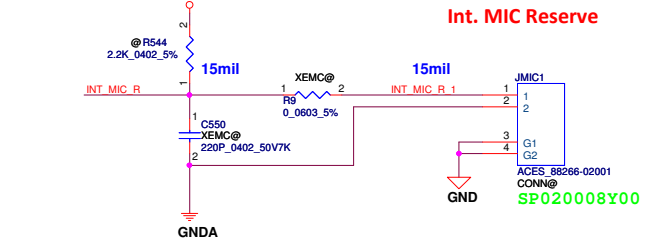
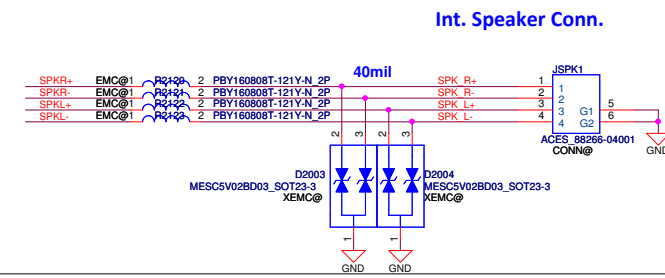
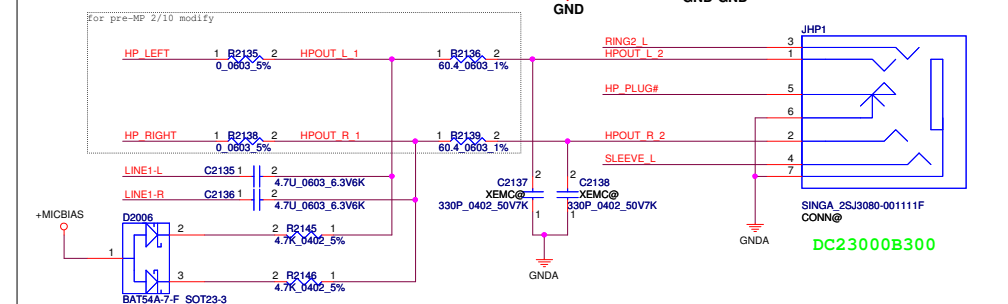
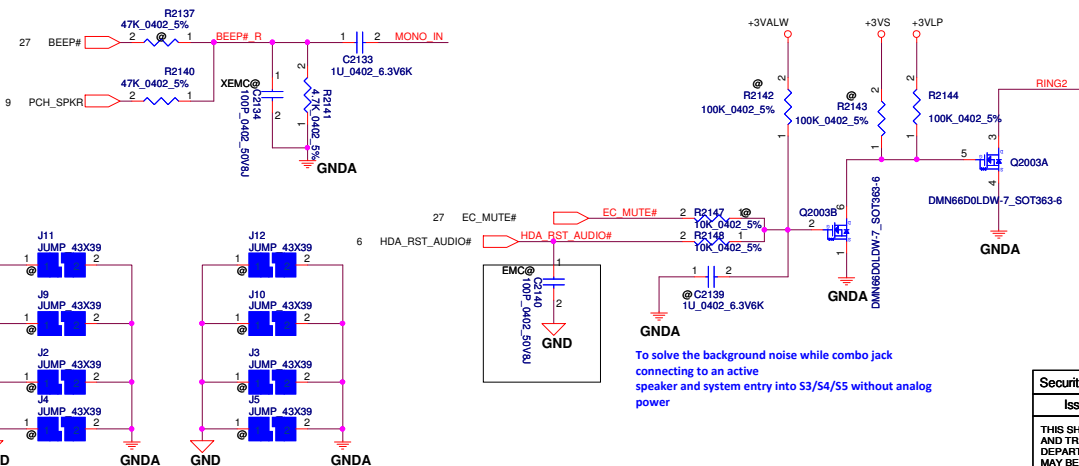
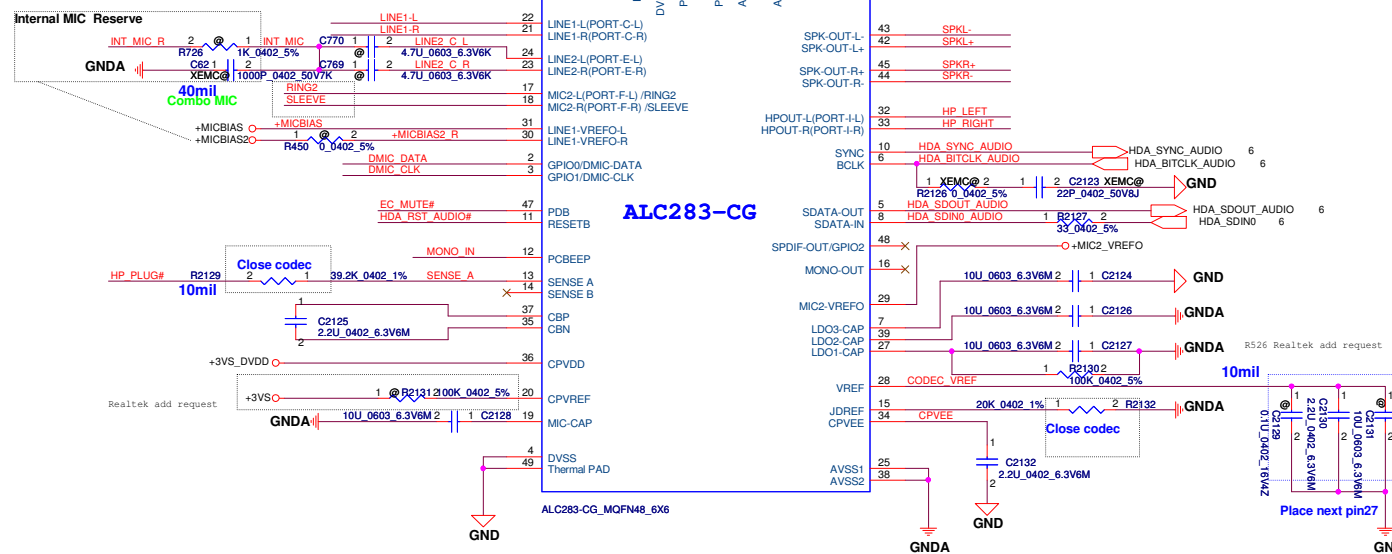
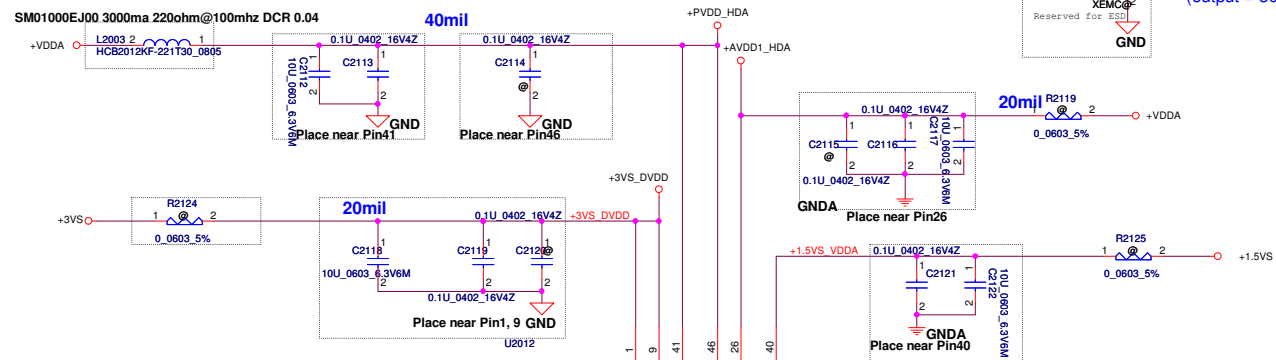


ON/OFF BTN



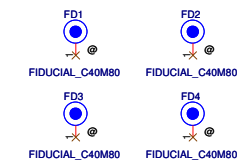
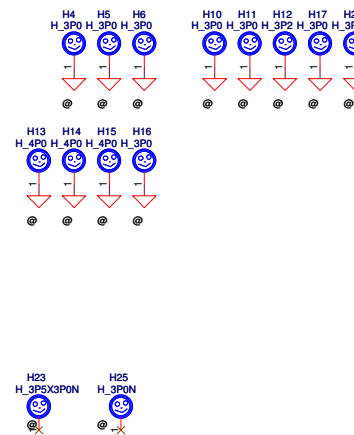
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Customer		Document Number		Rev	
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HD Audio Codec

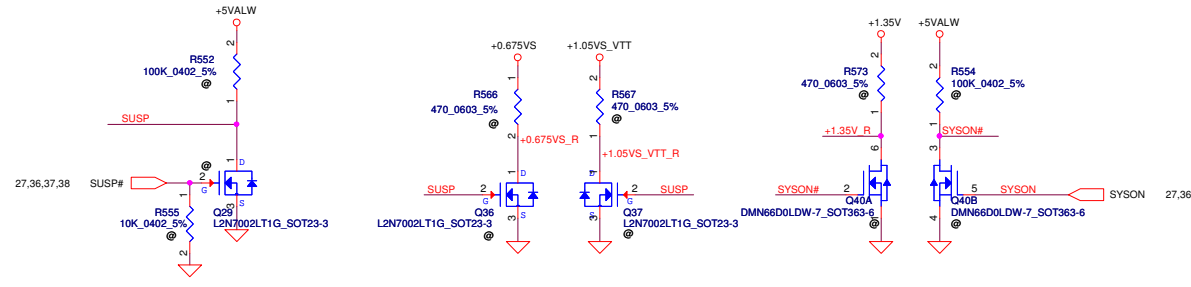
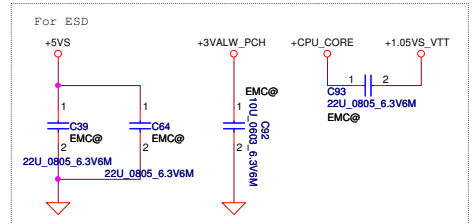
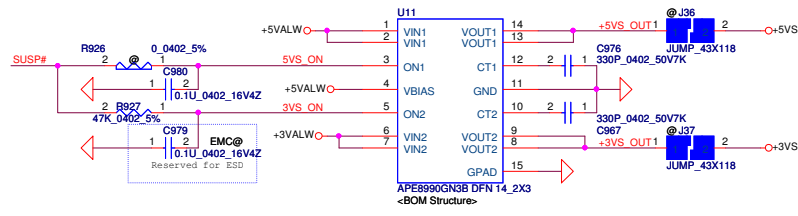


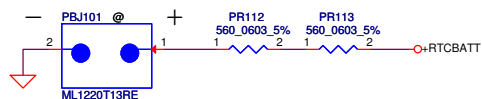
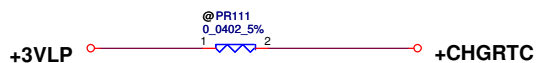
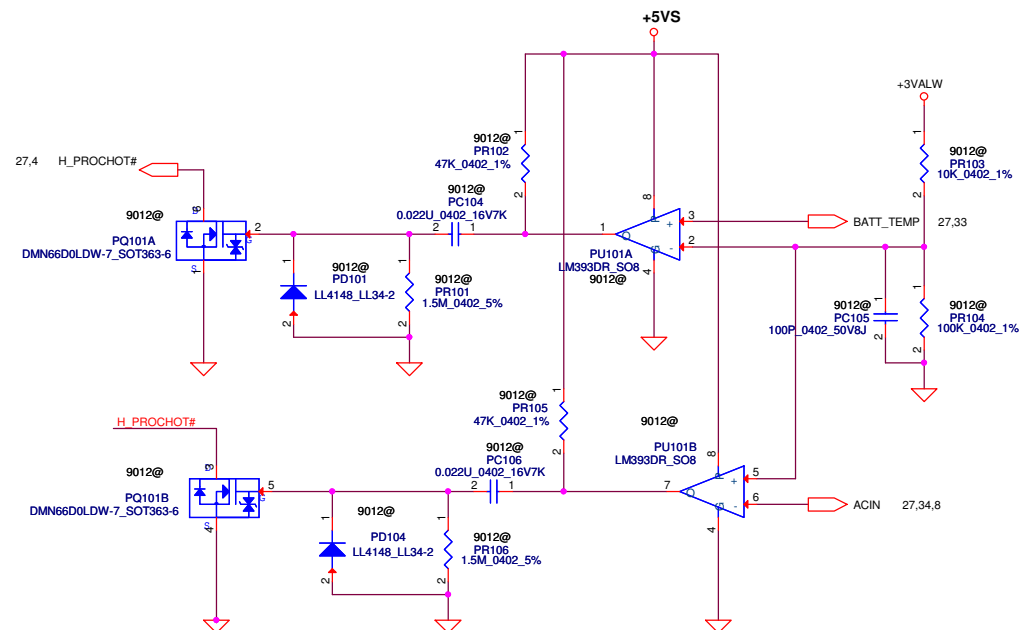
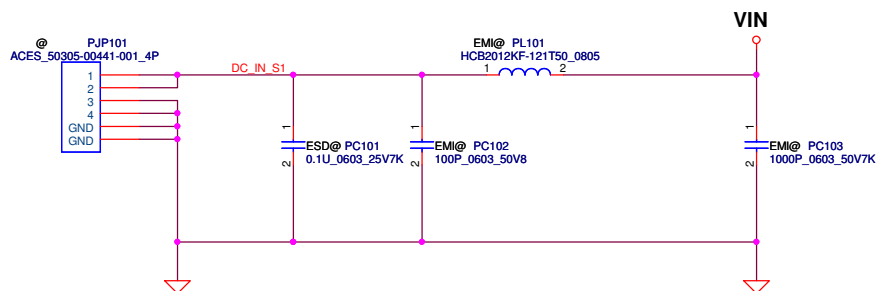
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Screw Hole

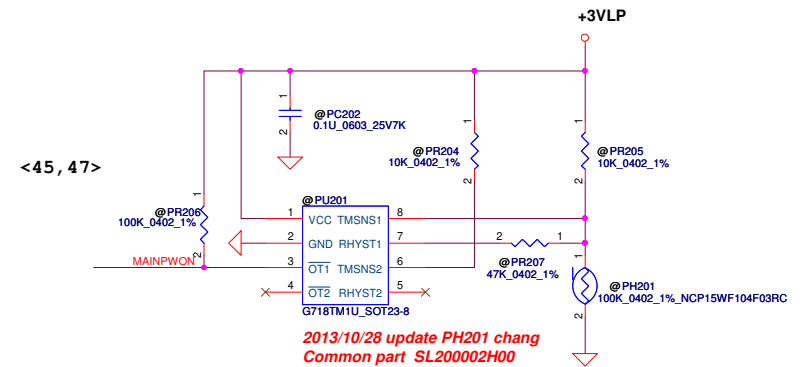
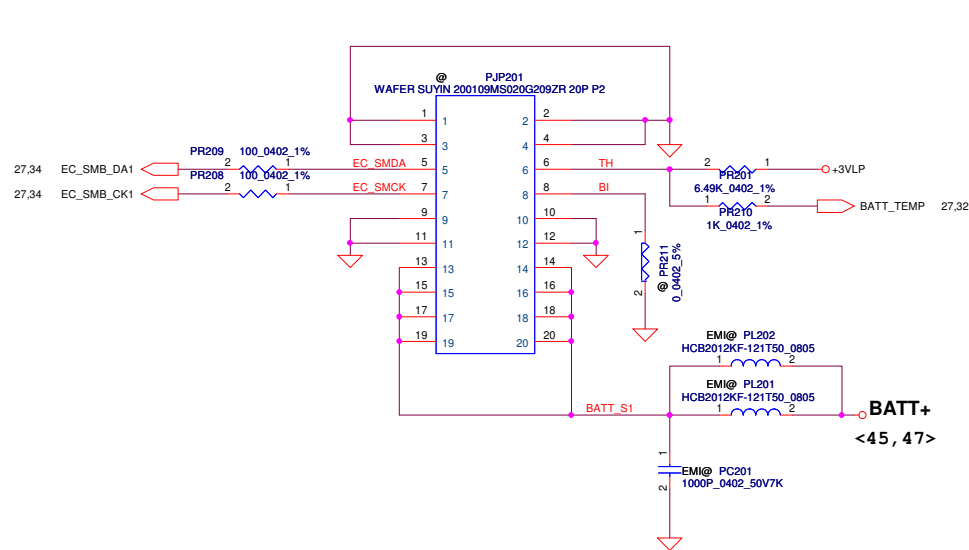
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---Battery_pin define---

PIN1 GND
PIN2 GND
PIN3 SMD
PIN4 SMC
PIN5 TS
PIN6 B/I
PIN7 Batt+
PIN8 Batt+

---Battery Con_pin define---

PIN8 GND
PIN7 GND
PIN6 SMD
PIN5 SMC
PIN4 TS
PIN3 B/I
PIN2 Batt+
PIN1 Batt+

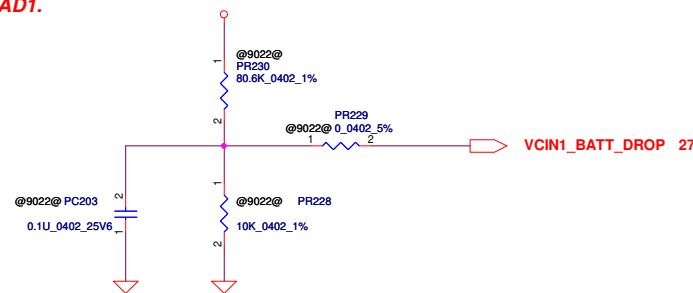
2013/10/14 update

For KB9022 sense 20mΩ	Active	Recovery
40W PR202 10K ohm	52W, 0.54V	40W, 0.42V
65W PR202 22.6K ohm	84.5W, 0.54V	65W, 0.42V

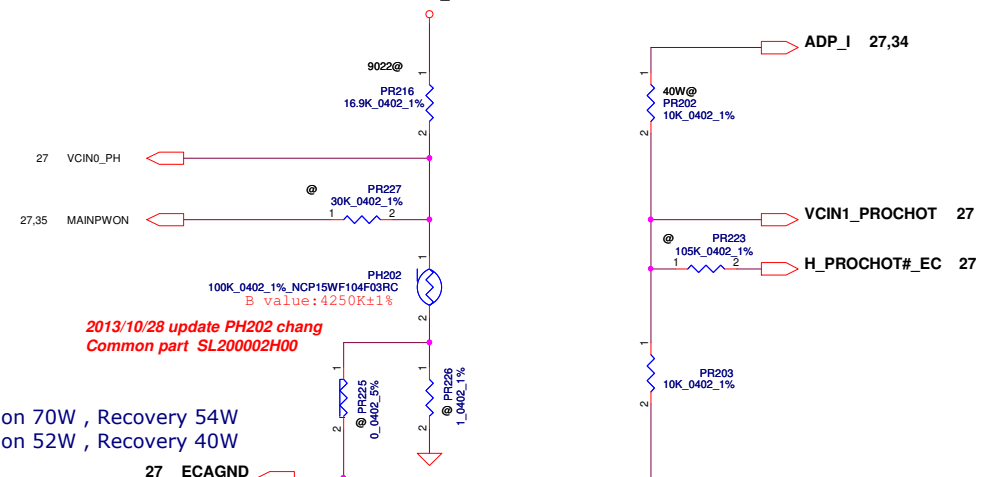
PH201 under CPU bottom side :
CPU thermal protection at 92 degree C (shutdown)
Recovery at 56 degree C

2013/10/02
Add for ENE9022 Battery Voltage drop detection. B+
Connect to ENE9022 pin64 AD1.

Battery is 3-cell design.
B+=9V



+EC_VCCA

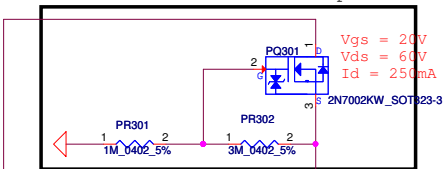


For 65W adapter==>action 70W , Recovery 54W
For 40W adapter==>action 52W , Recovery 40W

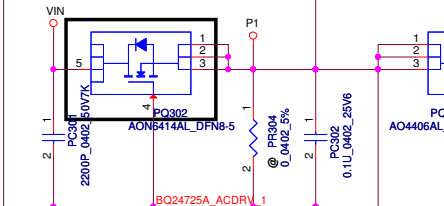
2013/10/28 update PH202 chang
Common part SL200002H00

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								Size		Document Number				Rev	
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Protection for reverse input



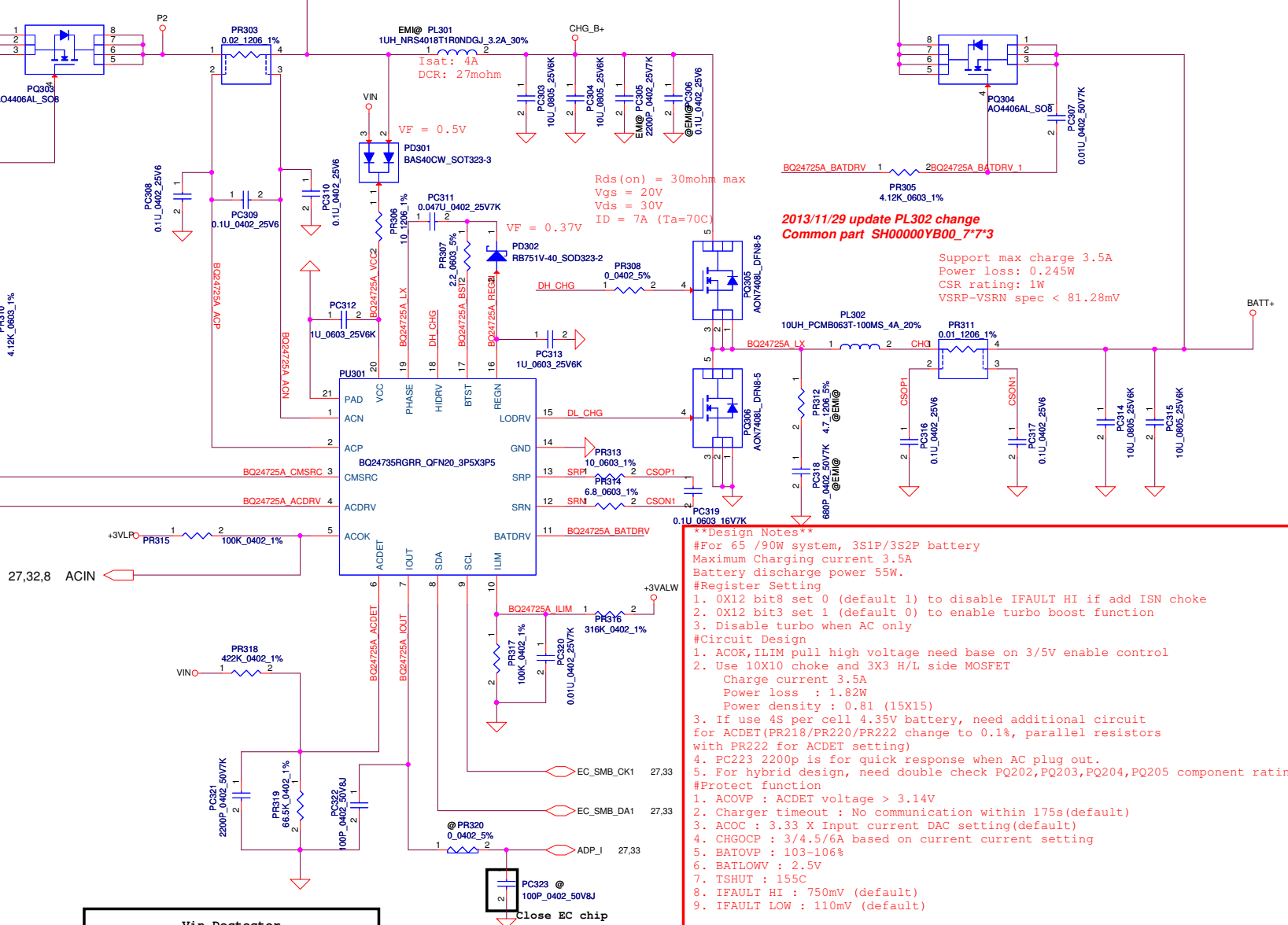
Need check the SOA for inrush



Module model information
BQ24735A_V1.mdd
BQ24735A_V2.mdd

2013/10/14
PR303 10m ohm chang -->20m ohm
SD00000S120

2014/01/21 update PL301 change
Common part SH00000YG00



Vin Detector			
Min.	Typ	Max.	
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

VILIM = 20*ILIM*Rsr
ILIM = 3.3*100/(100+107)/20/0.02
= 3.986 A

****Design Notes****
#For 65 /90W system, 3S1P/3S2P battery
Maximum Charging current 3.5A
Battery discharge power 55W.
#Register Setting
1. 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke
2. 0X12 bit3 set 1 (default 0) to enable turbo boost function
3. Disable turbo when AC only
#Circuit Design
1. ACOK, ILIM pull high voltage need base on 3/5V enable control
2. Use 10X10 choke and 3X3 H/L side MOSFET
Charge current 3.5A
Power loss : 1.82W
Power density : 0.81 (15X15)
3. If use 4S per cell 4.35V battery, need additional circuit for ACDET (PR218/PR220/PR222 change to 0.1%, parallel resistors with PR222 for ACDET setting)
4. PC223 2200p is for quick response when AC plug out.
5. For hybrid design, need double check PQ202, PQ203, PQ204, PQ205 component rating
#Protect function
1. AC0VP : ACDET voltage > 3.14V
2. Charger timeout : No communication within 175s(default)
3. ACOC : 3.33 X Input current DAC setting(default)
4. CHGOCP : 3/4.5/6A based on current current setting
5. BATOVLP : 103-106%
6. BATLOWV : 2.5V
7. TSHUT : 155C
8. IFAULT HI : 750mV (default)
9. IFAULT LOW : 110mV (default)

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								Common Circuit			
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SY8208B_V2.mdd
SY8208C_V2.mdd

ENLDO_3V5V



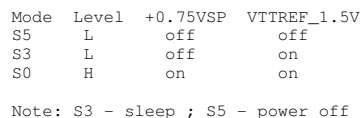
```
EC VDD0 is +3VL, PC426 UNPOP
EC VDD0 is +3VALW, PC426 POP
```

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RT8207M_V1.mdd	For Single layer
RT8207M_V2.mdd	For Dual layer

RT8207M_V1.mdd	For Single layer
RT8207M_V2.mdd	For Dual layer

0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A



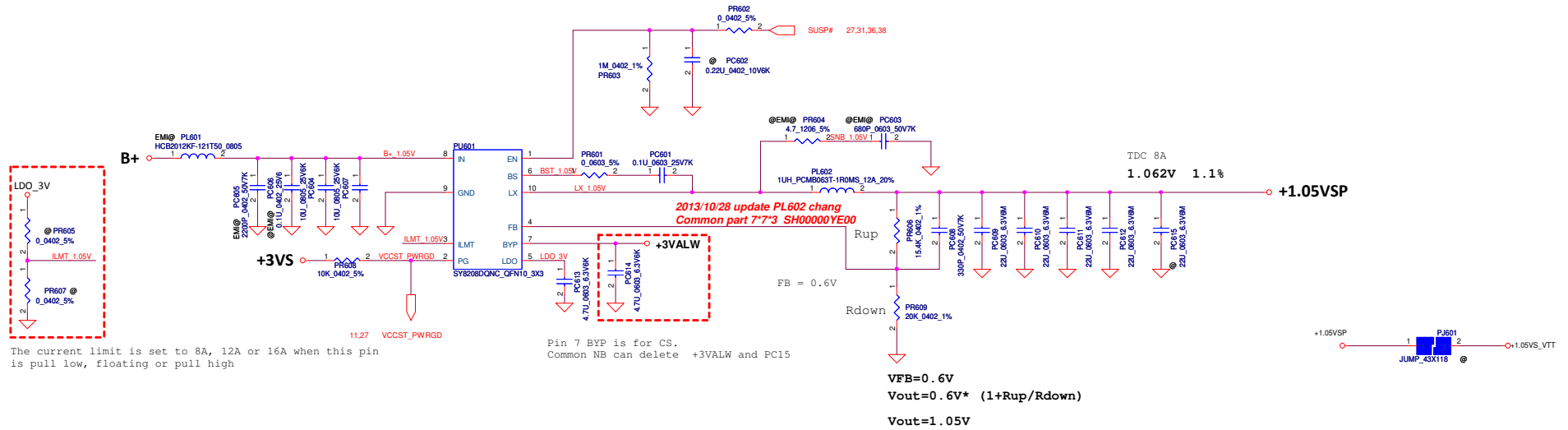
Switching Frequency: 285kHz
Ipeak=10A
Iocp~13A
OVP: 110%~120%
VFB=0.75V, Vout=1.515V
MOSFET footprint: SIS412DN

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Module model information

SY8208D_V1.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



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Module model information:
ISL95813 (for 15W & 28W CPU)

Base on BDW PDDG Rev_0_73			
Location	15W	28W	Note
	TDC 14A	TDC 19A	
	MAX 32A	MAX 40A	
	OCp 38.4A	OCp 48A	
	Loadline=-2.0mv/A	Loadline=-2.0mv/A	
PR820	392 Ohm	449 Ohm	OCp
PR816	1.27kOhm	1.58kOhm	Droop
PC816	0.033uF	0.022uF	RC Match
PR804	90.9kOhm	113kOhm	PROG1
PR807	93.1kOhm	95.3kOhm	IMON
PC811	0.1uF (0402)	0.1uF (0402)	RC Filter

L-side MOS: MDU1511RH
Rds(on):
<2.4mohm@Vgs=10V
<3.3mohm@Vgs=4.5V
Id :100A@Vgs=10V

-->20130828
Choke: 0.15UH (Size:7*7*4)
SH00000U300
Rdc=0.66mohm +-7%
Heat Rating Current=36A
Saturation Current=45A

Note:
VR_SVID_ALRT# Pull high on HW side

Note:
VR_HOT# Pull high on HW side

Over temperature protection:
OTP Setting: 100C active
Pin5 (NTC) voltage <0.88V, Protect
Pin5 (NTC) voltage >0.92v, recovery

2013/10/28 update PH802 chang
Common part SL200002E00

2013/12/12 update PL802 change

Common part SH000011H00

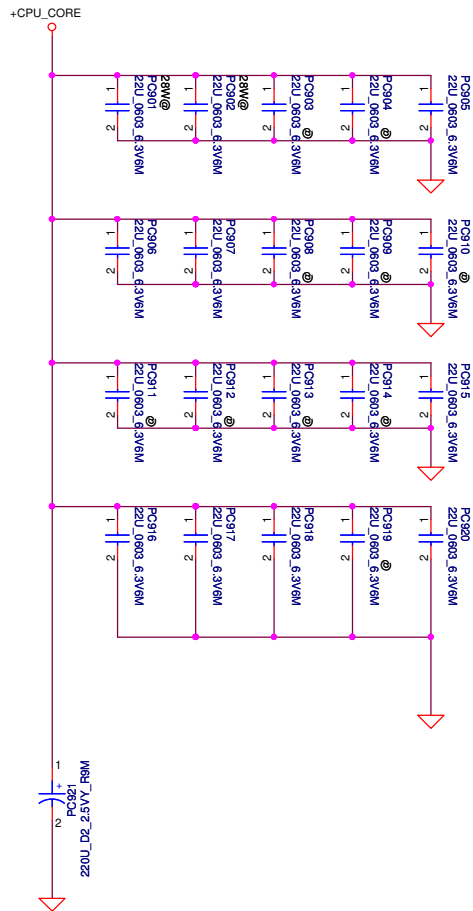
Height 8 mm
100u_SF000000I80

Height 6 mm
68u_SF000000W00

TDC 19A
MAX 40A
OCP 48A
Loadline=-2.0mv/A

Local sense put on HW site

PWR Rule
需確認最新SPEC.
Modify 8/6.



```
30 X 22uF 0805
2012/10/23
check the output cap Qty!!!
2012/10/24
23 pcs 22uF and reserve 7 pcs
2013/01/14
22uF*17      unpop:22uF*3
```

20130828
15W: 22uF*14
28W: 22uF*16

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Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
1	Design Update		P.35 P.37 P.37 P.39 P.34 P.33	Add unpop PC428 PC427,22U_0603_6.3V6M_SE00000M000 Add unpop PC615,22U_0603_6.3V6M_SE00000M000 PC609 PC610,SE00000PL00 change to 0603_6.3V6M_SE00000M000 PL801 PC807,Swap positions. PL302,10uH_10104_SH000005Z80 change to 10uH_773_SH00000YB00 Add PL202_SM01000C000	11/29	EVT
2	Design Update		P.35	PR410 R-short change to PD401_SCS00000Z00	12/09	EVT
3	Design Update	CPU Transient Test	P.39 P.40 P.40 P.40 P.33	PL802_SH00000U300 change to Common part SH000011P00 PC906 PC910 PC915 22U_0603_SE00000M000 SMT PC901 PC902 22U_0603_SE00000M000,SMT change to 28W@ PC916 PC915 22U_0603_SE00000M000 ,28W@ change to SMT PR227_30.9K_0402_1%_SD034309280 change to_30K_0402_1%_SD034300280	12/12	EVT
4	Design Update	CPU Transient Test		PR820_348_0402_SD00000EI80 change to 357_0402_SD034357080 (28W) PR820_348_0402_SD00000EI80 change to 316_0402_SD000003480 (15W) PR814_2K_0402_1%_SD034200180 change to unpop PC814_330P_0402_50V7K_SE074331K80 change to unpop PR813_5.9K_0402_SD034590180 change to 1.91K_0402_SD000009080 PR807_95.3K_0402_1%_SD034953280 change to 113K_0402_SD034113380 (28W) PR807_95.3K_0402_1%_SD034953280 change to 121K_0402_1%_SD034121380 (15W) PR817_Unpop change to 4.99M_0402_SD00000VO00	12/13	EVT
5	Design Update	VCINO VCIN1 B/I PIN Pull down Update Common part CPU Transient Test		PR211_1K_0402_SD034100180 Change to 0_0402_SD028000080 PR227_30K_0402_1%_SD034300280 change to unpop. PR216_32.4K_0402_1%_SD034324280 change to 16.9K_0402_1%_SD034169280 PR223_105K_0402_1%_SD034105380 change to unpop. PR202_10.5K_0402_1%_SD034105280 change to 10K_0402_1%_SD034100280 PQ303 PQ304 AON4466_SB00000CG80 --> AON4406_SB00000I800 PL301_1UH_SH00000MW00 --> 1UH +-30% 2.8A_SH00000YG00 Add PC426_4.7u_0402_SE00000SO00 15W:PR804_169K_0402_1%_SD034169380 --> 90.9K_0402_1%_SD034909280 28W:PR804_205K_0402_1%_SD034205380 --> 113K_0402_1%_SD034113380 PL802 0.15UH 20%_SH000011P00 -->0.22UH_20%_SH000011H00 15W:PR820_316_0402_1%_SD000003480 --> 392_0402_1%_SD00000F080 28W:PR820_357_0402_1%_SD034357080 --> 499_0402_1%_SD034499080 Add PC921_220U_D2_2.5VY_R9M_SGA00009800 Un pop PC903 PC904 PC908 PC909 PC9010 PC912 PC913 PC914 PC919	2014/ 01/21	DVT
15	Design Update	Update Common part		PR211 SD028000080 change to R-short PD401 SCS00000Z00 change to PR410 R-short	2014/ 02/17	PVT
16						
17						

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Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
1	Module Design	Module Design change 3/5V solution	3/5V	Un-pop PR1	11/13	DVT
2						
12						
13						
14						
15						
16						
17						

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Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
1		extra cap	24	unpop C165	1107	DVT
2	Desidn change	change EC board ID	27	AD_BID0 > change R506 to 12K POP R503	1107	DVT
3	Desidn change	change net "LINE1-L/LINE1-R" cap material	29	change C2135,C2136 to 4.7u 0402 to 0603	1107	DVT
4	Desidn change	modify ON/OFFBYN# circuit	27,28	DEL D24 , ON/OFF change to ON/OFFBTN#	1112	DVT
5	Desidn change	change CRT RGB bead material	21	change L2503,L2504,L2505 to 0402 bead(SM01000FH00)	1112	DVT
6	Desidn change	change +EC_VCCA ,EC_GND bead material	27	change L31 L32 to SM010009U00	1112	DVT
7	Desidn change	change USB port assign	18	Change USB port6 for CCD , Change USB port5 for TS	1112	DVT
8	Desidn change	change USB port assign	26	Change USB port7 for CR(USB)_FP	1112	DVT
9	Desidn change	reserve RTCRST# to EC	27	reserve RTCRST# to EC pin 27 for clear CMOS	1115	DVT
10	Desidn change	reserve RTCRST# to EC	28	add Q52 R490 reserve to EC RTCRST#	1115	DVT
11	Desidn change	share ROM function	7	POP R498,R500,R502,R505 for share ROM	1115	DVT
12	Desidn change	option LVDS EDID/EDP touch	18	change R438,R439,R415,R433 for option LVDS EDID/EDP touch	1115	DVT
13	Desidn change	EC_SMB_DA2	17	change to EC_I2C_TPDAT	1118	DVT
15	Desidn change	EC_SMB_CK2	17	change to EC_I2C_TPCLK	1118	DVT
16	Desidn change	RTD2132 EP_MODE	27	Add R491 reserve for RTD2132 EP_MODE	1118	DVT
17	Desidn change	change TP POWER	28	Change TP power to +3VALW	1118	DVT
18	CRT leakage	CRT_DATA/CRT_CLK add level shift	20	add R2502,R2503,Q2501 for level shift	1126	DVT
19	CRT leakage	change CRT POWER from 5VS to 3VS	20	add R2549	1126	DVT
20	CRT leakage	change CRT POWER from 5VS to 3VS	20	change pin PCSDA,PCSCL to +3VS_6513	1126	DVT
21	CRT leakage	change CRT POWER from 5VS to 3VS	20	change pin MCUVDDH to +3VS_6513	1126	DVT
22	Desidn change	change T/P int net connection support S3 wake	28	Change Q51 to D22 ,TP_INT# ,POP R633,del R452	1126	DVT
23	Desidn change	change EC_PME# pull up	22	add R2550 pull up to +3VLAN	1128	DVT
24	Desidn change	change EC_PME# pull up	27	unpop R484	1128	DVT
25	Desidn change	solve ESD	19	add C413 to +3VS	1204	DVT
26	Desidn change	solve ESD	29	add C2140,C2142,R2149,R2150	1205	DVT
27	Desidn change	solve ESD	29	change D2008 package	1205	DVT
28	Desidn change	ME drawing change	30	Del H9	1205	DVT
29	Desidn change	solve EMI	26	add R459,R460,R462,R463,L7,L8 for EMI request	1206	DVT
30	Desidn change	Change part number	18	change U22 PN	1209	DVT
31	Desidn change	Change part number	11	change C18 to SF000006S00	1209	DVT
32	Desidn change	Change part number	12	change C408 to SF000006R00	1209	DVT
33	Desidn change	Change part number	15	change C118 to SF000006S00	1209	DVT
34	Desidn change	Change part number	26	change C486 to SF000006R00	1209	DVT
35	Desidn change	Change part number	6	change C153 to 15pF to SE071150J80	1210	DVT
36	Desidn change	Change part number	7	change C2,C3 to 15pF to SE071150J80	1210	DVT
37	Desidn change	Change part number	22	change C2558,C2559 to 10pF to SE071100J80	1210	DVT
38	Desidn change	Change part number	29	change R2135,R2138 to 59 Ohm 0603	1210	DVT
39	Desidn change	solve EMI	29	change R2149,R2150 to SM01000NA00	1210	DVT
40	Desidn change	solve ESD	29	change C2142 , C2143 to 680pF	1210	DVT
41	Desidn change	Change part number	28	change SW to SN100000K00	1210	DVT
42	Desidn change	TP leakage from change TP VCC	28	add R452,R459,R460	1211	DVT
43	Desidn change	Change part number	23	change D1 to SCA00002M00	1216	DVT

Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
44	Desidn change	LAN Chip GPO	22	reserve R2551 0 ohm +3VALW to +3VLAN	1231	PVT
45	Desidn change	LAN Chip GPO	22	add R2540 (0 - Ohm) for disable PHY	1231	PVT
46	Desidn change	change CRT POWER from +5VS_6513 to +HDMI_5V_OUT	21	change CRT POWER from +5VS_6513 to +HDMI_5V_OUT	1231	PVT
47	Desidn change	TP PWR	27/28	unpop R459,add C2563,C2562,U2507 , add net "TP_PWR_EN" to EC pin 98	0110	PVT
48	Desidn change	TP connector	28	change connector type	0110	PVT
49	Desidn change	TS change to I2C0	09	change PCH GPIO4/GPIO5 to PCH_I2C0_SDA/PCH_I2C0_SCL	0110	PVT
50	Desidn change	TS change to I2C0	09	Del RP24 pin5 pin6 ,Add R276,R277 for TS I2C	0110	PVT
51	Desidn change	TS change to I2C0	18	change PCH_I2C1_SDA/PCH_I2C1_SCL to PCH_I2C0_SDA/PCH_I2C0_SCL	0110	PVT
52	Desidn change	R-Short		follow ZACH list	0110	PVT
53	Desidn change	solve ESD	15/29/27	add C35/C2140/C63 ,reserve C65/C68	0113	PVT
54	Desidn change	change USB CAP to 150U D2 size	26	change C486 to D2 150uF	0113	PVT
55	Desidn change	change LED brightness	28	change R699/R700 to 330 Ohm ,R698/R701 to 560 Ohm	0114	PVT
56	Desidn change	change Board ID to 0.3	27	change R506 to 15K (board ID)	0114	PVT
57	Desidn change	Change part number	29	change R2135,R2138 to 60.4 Ohm 0603	0114	PVT
58	Desidn change	Change TPM from module to on board	7	change R395 to TPM@	0115	PVT
59	Desidn change	Change TPM from module to on board	8	del net "LPCPD#" , reserve U2600,R2600,R2601,C2600,C2601,C2602,C2603,C2604,C2605 for TPM , R2603,C2606 for EMI , R2602 > @	0115	PVT
60	Desidn change	Change TPM from module to on board	28			
61	Desidn change	solve ESD	27	POP C509 EMC@	0116	PVT
62	Desidn change	solve epson crystal issue	22	add R2552	0116	PVT
63	Desidn change	solve EMI	29	change R2120,R2121,R2122,R2123 to bead SM01000CC00	0116	PVT
64	Desidn change	solve EMI	4	add C2144	0117	PVT
65	Desidn change	R-Short	11	change R126 to 0 - short	0120	PVT
66	Desidn change	Add Toch pad PS2 BUS level shift(solve PS2 leakage)	28	add R2509,R2507,R462,R463 reserve Q2502	0122	PVT
67	solve jack BO noise	solve audio BO noise sync with other project	29	change R2136/R2139 to 60.4 Ohm , R2135,R2138 to 0 Ohm	0210	pre-MP
68	Desidn change	modify DMIC net	29	delete R457	0213	pre-MP
69	Desidn change	reserve +3.3V for touch screen	18	add R82	0217	pre-MP
70	Desidn change	change +3.3V for touch screen	18	pop R82 , unpop R81	0218	pre-MP
71			28	unpop SW4	0218	pre-MP
72	Desidn change	change EC board ID to 1.0	27	change R506 to 20K Ohm	0224	pre-MP
73	Desidn change	change LED brightness	28	change R699/R700 to 200 Ohm ,R698/R701 to 390 Ohm	0304	pre-MP

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